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Atom-resolved imaging with a silicon tip integrated into an on-chip scanning tunneling microscope

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Limited throughput is a shortcoming of the Scanning Tunneling Microscope (STM), particularly when used for atomically-precise lithography. To address this issue, we have developed an on-chip STM based on Microelectromechanical-Systems (MEMS) technology. The device reported here has one degree of freedom, replacing the Z axis in a conventional STM. The small footprint of the on-chip STM provides a great opportunity to increase STM throughput by incorporating a number of on-chip STMs in an array to realize parallel STM. The tip methodology adopted for the on-chip STM presented here, which is a batch-fabricated Si tip, makes our design conducive to this goal. In this work, we investigate the capability of this on-chip STM with an integrated Si tip for STM imaging. We first integrate the on-chip STM into a commercial ultrahigh-vacuum STM system and perform imaging with atomic resolution on par with conventional STMs, but at higher scan speeds due to the higher sensitivity of the MEMS actuator relative to a piezotube. The results attest that it is possible to achieve a parallel and high-throughput STM platform which is a fully batch-fabricated MEMS STM nanopositioner capable of performing atomic-resolution STM imaging.

I. INTRODUCTION

Since its invention in the 1980s[1], the Scanning Tunneling Microscope (STM) has been a formidable tool in nanotechnology. Comprised of a piezoelectric nanopositioner and an atomically sharp tip on a metallic probe, the STM can be used to capture atomic-scale topographic images from a conductive sample and perform nanolithography for atomic resolution patterning of a resist on a surface[2]. The atomic precision and ultrahigh resolution of the STM have given it applications in single-atom manipulation[3] and adsorption/desorption in the nanotechnology field[4]. Due to its precision, the STM is now also being used to fabricate atomic-scale devices, such as atomic switches[5], atomic wires[6], single-atom transistors[7], and solid-state quantum computers[8,9], to name a few.

A conventional STM operates by moving a nanometer-sharp tip within a few angstroms of a conductive surface with a three-degree-of-freedom (3-DOF) piezotube scanner. When a bias voltage is applied between the sample and tip, a tunneling current is established in the tip-sample gap due to a quantum mechanical phenomenon called tunneling. To control the tunnel current, a feedback loop with a proportional-integral controller is used to maintain the tip-sample distance by regulating piezotube movement in the Z axis. The magnitude of the tunnel current is extremely sensitive to the tip-sample distance so a Z resolution of a few picometers is achievable. Once the tunneling current has been established, an STM image is then constructed by raster scanning the tip over the sample with the piezotube. By plotting the controller output over the corresponding piezotube X and Y coordinates, a topographic image of the sample is obtained.

Unfortunately, the slow scanning speed of the STM has limited its widespread use, especially as a nanolithography tool, where, despite its superior precision and resolution, its throughput is far less than conventional electron-beam lithography [10]. Furthermore, the large size of the piezotube that scans the tip over the sample surface gives it a low bandwidth, limited to around $1\,kHz$[11,12]. The bulkiness of the piezotube has also resulted in most STM systems being comprised of a single tip instead of a multi-tip array configuration, which would increase the throughput.

As a way to improve the low throughput of the STM, we have replaced the slow Z axis of a conventional STM piezotube[13] with a 1-DOF Microelectromechanical-System (MEMS) nanopositioner. Due to its small mass, the MEMS nanopositioner increases the Z-axis bandwidth of the STM system up to $10\,kHz$ and maintains a stroke of $2\,\mu m$. In addition, its small footprint provides a great opportunity to employ an array of such MEMS devices to realize a highly parallel STM platform, which would be a giant leap for large-scale metrology or high-throughput nanolithography with atomic precision. The MEMS device also benefits from electrostatic actuators which make it immune to the well-known artifacts of piezoactuators, such as creep and hysteresis[14,15].

Earlier designs of the MEMS nanopositioner with Pt and W tips have demonstrated atomic-resolution imaging and lithography when the MEMS device is integrated into a commercial UltraHigh-Vacuum (UHV) STM [16,17]. However, the focused-ion-beam process of growing or welding these metal tips onto the MEMS device is slow and delicate, not suitable for scaling up to large arrays of tips. Therefore, fabricating STM tips using standard microfabrication processes has received much attention from the STM community[18].

We have further modified our previous design by integrat-

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ing an in-plane Si tip on the MEMS device that is suitable for batch fabrication[19]. In this paper, we demonstrate atomic-resolution imaging with this MEMS nanopositioner with the in-plane Si tip. This is a major step in proving the capability of a fully batch-fabricated MEMS device as an on-chip STM which can be extended into an array to achieve a highly parallel STM system.

The remainder of the paper is structured as follows. In Section II, we explore the viability of Si as an STM tip. Section III outlines the design and properties of the MEMS device with the integrated Si tip, while Section IV describes the hybrid system that is achieved by incorporating the MEMS device into a commercial UHV STM. The experimental results containing STM images obtained by different MEMS devices are then presented in Section V. Lastly, conclusions and future work are laid out in Section VI.

II. SILICON AS STM TIP

Metals, such as W or Pt-Ir alloy, have become the first choice for the tip material since the advent of the STM. Over the years, researchers working with Si samples discovered that images with enhanced atomic resolution are mostly obtained after a slight and controlled touch of the sample surface with the tip. Therefore, it has become a routine practice among STM operators to improve the image quality through this method when the tip is to blame. Further investigations show that such a procedure leaves a tip terminated with a Si atom at its end[20]. It is the Si atom at the apex of such a compound tip that plays the main role in enhancing the image quality. This empirical practice formed a basis for us to integrate a tip made of Si on our MEMS device. Analysis of the electronic structure of Si further confirms that a tip made of Si is capable of STM imaging with atomic resolution.

Corrugation amplitude and lateral resolution of STM images first and foremost depend on the geometry and properties of the tip. The origin of atomic resolution imaging lies in the existence of localized surface states. Atomic resolution imaging cannot be achieved if neither the tip nor the sample consists of a localized state on its surface. Therefore, to ensure atomic resolution, only two groups of materials can be used as an STM tip[21]. The first group is the d-band metals where the majority of their Fermi-level states are d-type states. For instance, the widely used tip material, W, is known to form d_{z^2} states on its surface. The second group is certain semiconductors that form p_z-like states on their surface. This includes Si which tends to form localized sp^3 states on its surface[22].

Although semiconductor tips are not common in scanning tunneling microscopy, they can have certain advantages over their metallic counterparts. First, an STM tip made of a direct band-gap semiconductor can be used as a source of spin-polarized tunneling electrons to study the magnetic properties of a sample instead of a ferromagnetic tip[23]. Moreover, batch fabrication processes have already been developed in the semiconductor industry for materials such as Si, which makes it an ideal candidate for an integrated tip on a MEMS device.

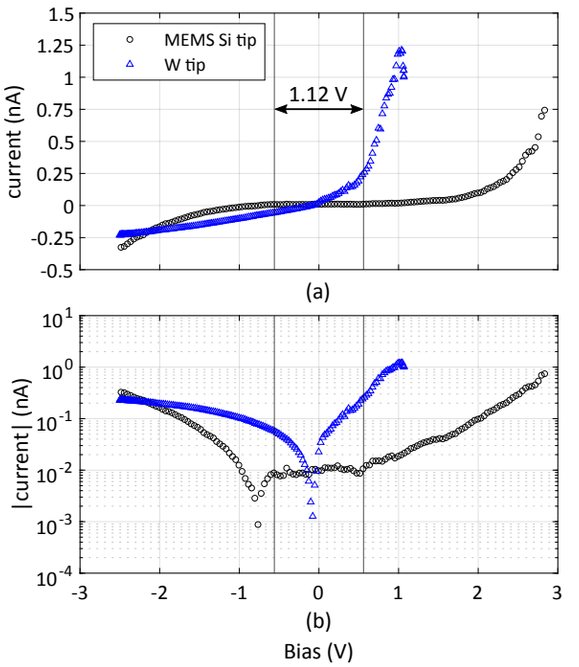

FIG. 1. I/V curves obtained with a MEMS Si tip device and a regular STM W tip: (a) linear and (b) logarithmic displays.

However, it is worth noting that there exists a 1.12-eV band gap in the energy levels of Si. For an STM tip made of intrinsic Si, this would necessitate a bias voltage of at least half of this gap to establish a tunnel current. Since our MEMS device with an integrated Si tip is fabricated from highly n-type doped Si, its Fermi level lies near the conduction band, and as a result, we do not expect its band gap to hinder the MEMS Si tip from establishing a tunnel current.

Fig. 1 presents variations of the tunnel current versus sample bias when the tip is kept at a constant distance from a sample. For this, we utilize the experimental setup described in Section IV to establish a tunnel current with a MEMS device on a H-passivated Si (100)-2×1 surface. Then, the feedback loop is turned off while keeping the tip-sample gap constant. Then, the tunneling current value for various sample biases is measured to provide a spectroscopic I/V curve, which is plotted in both linear and logarithmic displays in Fig. 1. In this process, the tip stays motionless close to the sample surface, which can be a challenging task for a piezotube with a creep artifact but is seamless thanks to the creep-free electrostatic actuation methodology incorporated in the MEMS device.

Even though the band gap cannot prevent the MEMS Si tip from establishing a tunnel current, its effect appears in the I/V curve. The nonuniform Density of States (DOS) of Si, as the tip material, can indeed cause misinterpretations when measuring the DOS of a sample. For comparison, a similar I/V curve with a regular STM W tip mounted on the piezotube is obtained and included in Fig. 1.

When a negative bias is applied to the sample, electrons tunnel from the occupied states of the sample into the empty

states of the tip. If the tip is metallic with uniform DOS, the electronic properties of the filled states of the sample can then be probed by sweeping the bias in the negative region. As evident from Fig. 1 a, we observe a linear trend in the I/V curve in this region when the W tip is used which is indicative of a metallic characteristic. On the other hand, when a positive bias is applied to the sample, electrons tunnel from the occupied states of the tip into the empty states of the sample. Then, by sweeping the bias in this positive region and again assuming a uniform DOS for the tip, electronic properties of the empty states of the sample can be revealed. Therefore, the trend in the positive region of the I/V curve when using the W tip presents the electronic properties of the filled states of the H-passivated Si surface.

In the case of the MEMS Si tip, we observe that the electrons tunnel into the conduction band of Si for the biases less than -0.76 V, as is clear from its I/V trend in Fig. 1 b. When increasing the bias from -0.76 V towards positive values, we first observe an initial increase in the current which, this time, comes from the electrons tunneling out of the conduction band of the Si tip and into the empty states of the sample. This proves that the Fermi level of the MEMS Si tip indeed lies inside its conduction band. After this initial increase, the current encounters a rather stagnant region for the biases between -0.56 V to 0.55 V. This is where the band gap of the Si tip enters the bias window which hinders the increase in the current since there is no state in the band gap region. Above 0.55 V, electrons in the valence band of the Si tip now start tunneling into the empty states of the sample. This band gap effect along with the fact that Si, as a semiconductor material, possesses nonuniform DOS causes the I/V trend obtained with the MEMS Si tip to differ from the one obtained with the W tip. This would make extraction of the sample electronic properties with the MEMS Si tip challenging. For the sake of clarification, the 1.12-V gap region of bulk Si is also indicated in Fig. 1 which coincides with the stagnant region in the I/V curve obtained with the MEMS Si tip.

III. MEMS NANOPOSITIONER

We proposed a fully batch-fabricated 1-DOF MEMS device with an integrated Si tip in our previous work[19]. This device is intended to replace the Z axis of piezotubes in UHV STM systems. Therefore, it should provide the same range of motion as an STM piezotube along the Z axis, 1-2 μm, using a similar actuation voltage, 150 V.

To achieve this goal, a shuttle beam with one of its ends formed into an in-plane Si tip is employed in the MEMS device. Fig. 2 a presents a schematic of the MEMS device. The shuttle is suspended from a substrate with the help of 16 compliant double-clamped flexures and is equipped with 44 pairs of electrostatic parallel-plate actuators. The flexures are designed jointly with actuators to provide enough restoring force against the tip-sample attractive forces to prevent snap-in between the tip and sample while fulfilling the 2-μm range-of-motion requirement of the device with less than 150 V applied to the actuators. According to the finite element analyses, the

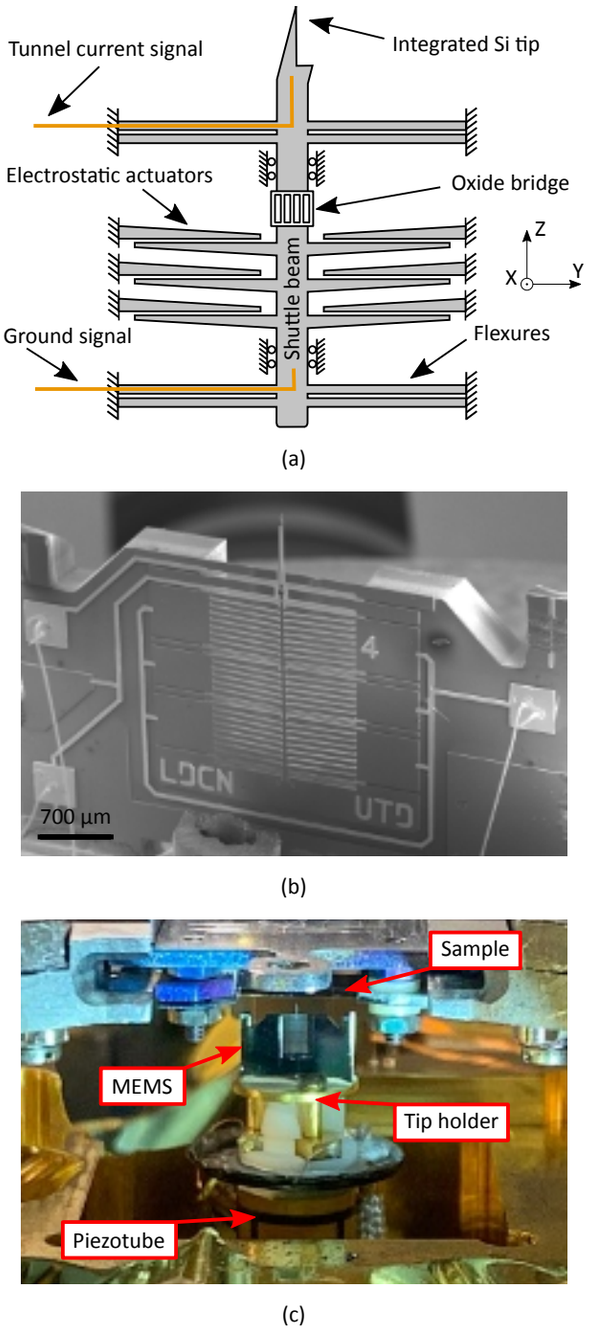

FIG. 2. The MEMS device with integrated Si tip: (a) a schematic of the device (b) An SEM image of the device (c) the MEMS assembly mounted onto the piezotube inside the UHV chamber.

total stiffness of the device along the axis of motion (Z axis in Fig. 2 a) is 285 N/m which corresponds to a displacement of 2.2 μm while applying 69.4 V to the actuators. The simulations also revealed that the first resonance of the device lies at 13.7 kHz along this axis, far higher than the 1 kHz of a piezotube.

The MEMS device is compatible with standard SOI batch

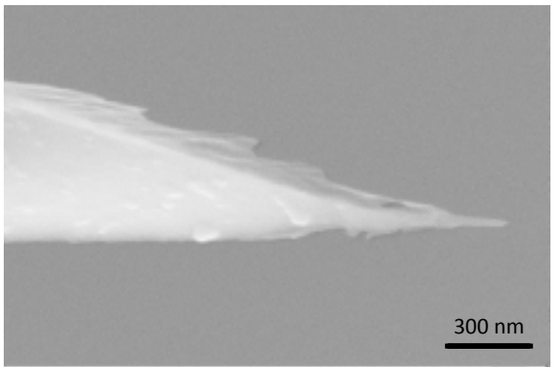

FIG. 3. An SEM image of the Si tip at the end of the shuttle beam of a MEMS device after FDSS sharpening.

fabrication processes available in a cleanroom environment. To provide enough conductivity for its integrated tip, the device is made from a highly doped silicon-on-insulator wafer (0.001-0.005 Ωcm, *n*-type, (100)) with a 20-μm-thick device layer. The in-plane tip at the end of the shuttle beam is formed by intersecting three planes in the device layer, resulting in a single point. One of these planes is the bottom side of the device layer. The second plane is perpendicular to the first one and is formed by a vertical dry etch of Si using the deep-reactive-ion-etch process. The last plane is the inclined (111) plane of Si which is attained by anisotropic wet etching of Si in KOH.

The complexity of the tip's fabrication necessitates having the shuttle beam connected to the tunneling and ground signals at the same time. Therefore, a novel scheme called the oxide bridge is developed to allow the shuttle beam to be composed of two electrically separated but mechanically connected sections, as in Fig. 2 a. The oxide bridge is based on having slender Si beams between the two parts of the shuttle for the mechanical connection. Thermal oxidation of the beams with a subsequent silicon oxide deposition brings electrical separation between the two parts while maintaining a mechanical connection. By using the oxide bridge, the front section of the shuttle where the tip is located is dedicated to the tunneling signal while the rest of it is grounded, as required for the actuators' functionality.

Fig. 2 b shows a Scanning-Electron-Microscopy (SEM) image of the 1-DOF MEMS STM nanopositioner with an integrated Si tip. Similar to the earlier design of the MEMS device with post-process tips[16], the current MEMS device also experiences a stiffening effect when glued using epoxy onto a tip holder. For instance, the first resonance of a device was initially measured to be 10.7 kHz which then increased to 21.5 kHz after the gluing, indicative of a four-fold increase in the stiffness of the flexures. This effect can be attributed to the the thermal process taking place in an oven which is necessary for curing the epoxy.

After epoxying the MEMS device onto a tip holder, we further sharpen the Si tip of the MEMS device using the Field-Direct-Sputter-Sharpening (FDSS) process[24]. This sharpening step also helps to reduce the amount of native oxide on the tip before introducing it into a UHV STM chamber. The apex of such a Si tip after FDSS sharpening is presented in Fig. 3.

IV. EXPERIMENTAL SETUP

To perform atomic-resolution STM imaging with the proposed MEMS device with an integrated Si tip, we utilize the hybrid system introduced in our previous work[16]. In this hybrid system, a 1-DOF MEMS device is incorporated into a commercial UHV STM system from ScientaOmicron to generate the Z axis motion during STM operations while the X and Y motions are provided by the system's piezotube. Fig. 2 c shows a MEMS assembly sitting on top of the system's piezotube inside the UHV chamber.

The whole hybrid system is operated with a commercial STM control system (ZyVector, Zyvex Labs LLC) which performs automatic tip landing and scanning. Additionally, its live position correction feature remedies the piezotube-related artifacts for the XY-plane motions, such as creep and hysteresis. These artifacts are averted along the Z axis due to the use of the MEMS device.

A matter of concern in our proposed hybrid system is the fragility of the MEMS devices when compared to their macroscopic counterpart,the piezotube. In our experience, there were few instances of the MEMS devices being compromised due to mishandling when transferring them inside the UHV chamber. However, after maturing the necessary skill set, we were able to routinely handle the devices without any incidents. After the MEMS assembly gets mounted onto the piezotube, the control system brings the MEMS closer to the sample in a controlled and safe manner, just as in the case of regular STM tips.

The sample used to perform imaging is an H-passivated Si (100)-2$\times$1 surface prepared under UHV conditions[16]. It is made of a 4$\times$10-mm^2 piece of low-doped Si (100) (1-10 Ωcm, *n*-type) whose surface is passivated with a monolayer resist, i.e. H atoms. This type of sample has attracted particular attention in the past few decades as it is frequently used as the basis for fabricating atomically precise nano-electronic devices[25].

V. EXPERIMENTAL RESULTS

Benefiting from the hybrid system, we can routinely land the tip on the sample surface without crashing it into the surface. A typical tunnel current established with the MEMS device along with the corresponding control command are presented in Figs. 4 a and b. Here, the MEMS shuttle is extended during the first twenty seconds until the tunnel current is established. The feedback loop implemented with the help of the control system keeps the tunnel current at a predefined setpoint by regulating the tip-sample gap for about two minutes until the MEMS shuttle is retracted. As in our previous work[16], the control command is passed through a square root function before applying it to the amplifier to linearize the quadratic relationship between the applied potential on the

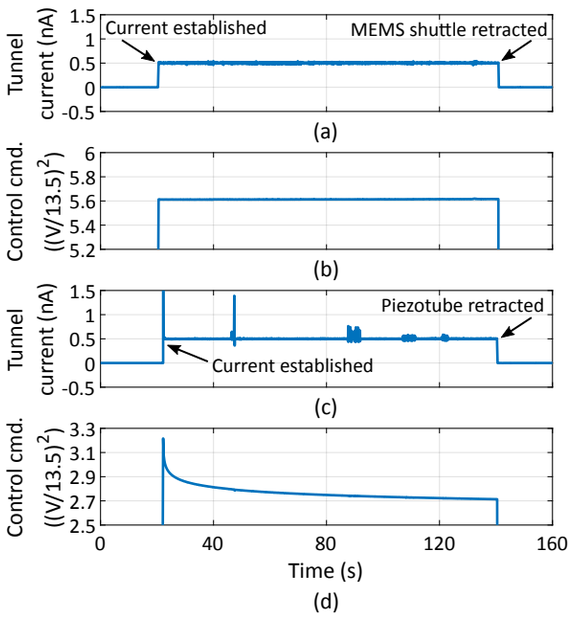

FIG. 4. Tunnel current establishing: (a) tunnel current signal and (b) corresponding control command signal when a MEMS device is used, (c) tunnel current signal and (d) corresponding control command signal when a regular STM W tip is used. For both tests, the bias and current setpoint are -3.5 V and 0.5 nA, respectively.

MEMS electrostatic actuators and the resulting electrostatic force.

For the sake of comparison, we present a similar tunnel current establishment with a regular STM W tip mounted on the piezotube in Figs.4 c and d. The standard deviation of the tunnel current signal for the MEMS device case is 5.7 pA, whereas this value for the W tip with the piezotube is 15.9 pA. The higher standard deviation with the W tip can be due the sporadic spikes visible in Fig. 4 c, otherwise we can conclude that the noise levels for both tips are comparable. It is also worthwhile to mention that no creep effect exists when using the MEMS device (Fig. 4 b). In the W tip case, on the other hand, the piezotube continues to creep even long after the tip has landed. The controller must then properly compensate for this creep, as evident in Fig. 4 d. For the W tip, a large overshoot in the tunnel current (up to about 3.12 nA, not shown in Fig. 4 c) occurred at the moment of landing.

Next, the piezotube rasters the MEMS tip in the XY plane, and the topography of the sample is constructed from the control command driving the MEMS shuttle. We tested four different MEMS devices with integrated Si tips in the hybrid system, and the resulting STM images are presented in Fig. 5. As is clear from these images, the rows of dimers of the H-passivated Si (100)-2×1 surface, comprising two Si atoms each bonded to an H atom, are clearly resolved. The dimer row directions perpendicular to each other at adjacent terraces are also visible. The bright spots, which are due to missing H atoms on the Si surface leaving unsatisfied dangling bonds of the underlying Si atoms, are distinguishable. In these atomic sites, the tunneling conductance increases, and as a result, the feedback loop retracts the tip to compensate for the increase in the tunneling signal. On the other hand, the black holes in the images are generated due to missing Si atoms in the lattice. Moreover, in Fig. 5 c, image quality is maintained at a scan speed of 625 nm/s, approximately three times the typical scan speed used with a standard piezotube scanner.

It is worthwhile to mention that just as in the case of regular STM tips, we also sometimes benefited from the controlled tip-sample touch technique to reshape the apex of the Si tip and improve the quality of the STM images obtained with the MEMS device. This capability is particularly important as it allows recovery of the MEMS Si tips, and as a result, increases the lifetime of the MEMS device. Besides the H-passivated Si surface, our MEMS Si tips also could withstand such controlled tip-sample touch procedure on an Au sample.

To assess the durability of the Si tip integrated into the proposed MEMS device, we scanned a spot on the H-passivated Si sample consecutively for about ten minutes, three images of which are presented in Figs. 5 d-f. As evident from these identical images, not only does the MEMS Si tip not alter the sample surface but also it maintains its integrity during imaging. With these results, the hybrid system benefiting from the MEMS device with the integrated Si tip proves to be capable of performing STM imaging on a par with conventional STM systems.

VI. CONCLUSION

This work demonstrated the capability of an on-chip STM with a batch-fabricated Si tip to carry out STM imaging on par with conventional STM systems. In this regard, we integrated 1-DOF MEMS STM nanopositioners with integrated Si tips into a commercial UHV STM system. As a result, a hybrid STM was achieved whose Z axis is delivered by the MEMS device, while its XY-plane motions are generated by the original system's piezotube. Stable STM imaging was performed with the hybrid system throughout the experiments.

In conclusion, the proposed 1-DOF MEMS-based STM nanopositioner with an integrated Si tip stands out as a promising candidate to be employed in a highly parallel MEMS-based STM platform for high-throughput scanning tunneling microscopy, as such a platform requires a large number of identical STM tips placed close to each other. As a future work, we will develop an array of 1-DOF MEMS nanopositioners based on this design to materialize parallel scanning tunneling microscopy. In addition, we will attempt to cover the Si tip of the MEMS devices with a metal layer using microfabrication processes in order to avoid the adverse effects of the Si band gap and its nonuniform DOS on the spectroscopic data. Furthermore, advanced control techniques will be implemented to further enhance the control performance of our hybrid system[26–28].

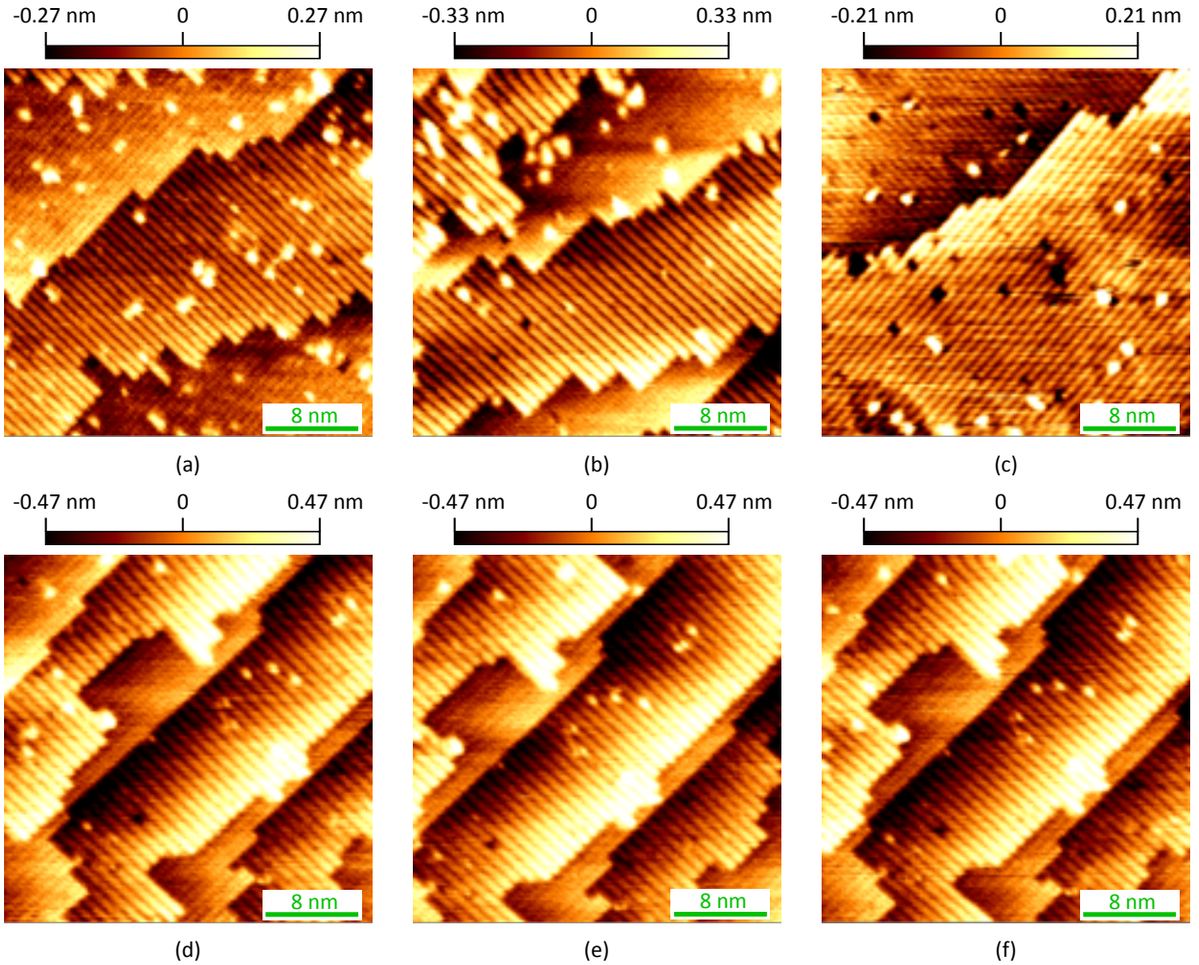

FIG. 5. STM imaging with the hybrid system with four different MEMS devices: (a-c) three images obtained with three different devices. (d-f) Three consecutive images of a spot on the sample obtained with the fourth device over ten minutes. The imaging parameters are as follows: (a) setpoint= 0.25 nA, scan speed= 201.6 nm/s (b) setpoint= 0.75 nA, scan speed= 312.5 nm/s (c) setpoint= 0.05 nA, scan speed= 625 nm/s (d-f) setpoint= 0.5 nA, scan speed= 312.5 nm/s. For all six images: bias= -3 V, scan size= 32 $nm \times 32$ nm, image resolution= 512×256 $pixels$.

VII. ACKNOWLEDGMENTS

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VIII. AUTHOR DECLARATIONS

A. Conflict of interest

The authors have no conflicts to disclose.

IX. DATA AVAILABILITY

The data that supports the findings of this study are available within the article.

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