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Improved Current and Charge Amplifiers for Driving Piezoelectric Loads, and Issues in Signal Processing Design for Synthesis of Shunt Damping Circuits

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ABSTRACT: Piezoelectric transducers are known to exhibit less hysterisis when driven with current or charge rather than voltage. Despite this advantage, such methods have found little practical application due to the poor low-frequency response of present current and charge driver designs. This paper introduces the *compliance feedback* current driver containing a secondary voltage feedback loop to prevent DC charging of capacitive loads and to compensate for any voltage or current offsets within the circuit. Low-frequency bandwidths in the milli-Hertz range can be achieved. One application for such a device is the synthesis of piezoelectric shunt damping circuits. A number of block diagram transformations are presented to simplify the realization of analog or digital admittance transfer functions from a schematic circuit diagram.

Key Words: current source, charge source, amplifier, driver, precision, shunt damping, synthetic admittance, synthetic impedance, transformations, implementation

INTRODUCTION

PIEZOELECTRIC transducers have found countless applications in such fields as vibration control (Hagood et al., 1990), nano-positioning (Croft et al., 2000), acoustics (Niezrecki and Cudney, 2001), and sonar (Stansfield, 1991). The piezoelectric effect (Jaffe et al., 1971; IEEE Standard on Piezoelectricity, 1987; Adriaens, 2000), is a phenomenon exhibited by certain materials where an applied electric field produces a corresponding strain and *vice versa*. The effect can be exploited in one, two, or three dimensions, for actuating, sensing, or sensori-actuating (Dosch et al., 1992). One common theme across the diverse literature involving piezoelectric applications is the problem of hysteresis (Jaffe et al., 1971; Adriaens, 2000). When used in an actuating role, piezoelectric transducers display a significant hysteresis in the transfer function from voltage to displacement (Jaffe et al., 1971; Adriaens, 2000).

As discussed in (Furutani et al., 1998) and references therein, a great number of techniques have been developed with the intention of reducing hysteresis. Included are displacement feedback techniques, mathematical Preisach modeling (Mayergoyz, 1991) and inversion, phase control, polynomial approximation, and current or charge actuation.

Almost all contributions in this area make reference to the well-known advantages of driving piezoelectric transducers with current or charge rather than voltage (Newcomb and Flinn, 1982). Simply by regulating the current or charge, a fivefold reduction in the hysteresis can be achieved (Ge and Jouaneh, 1996). A quote from a recent paper (Cruz-Hernandez and Hayward, 2001) is typical of the sentiment towards this technique:

> "While hysteresis in a piezoelectric actuator is reduced if the charge is regulated instead of the voltage (Newcomb and Flinn, 1982), the implementation complexity of this technique prevents a wide acceptance (Kaizuka and Siu, 1988)".

Although the circuit topology of a charge or current amplifier is much the same as a simple voltage feedback amplifier, the uncontrolled nature of the output voltage typically results in the load capacitor being charged up. Saturation and distortion occur when the output voltage, referred to as the compliance voltage, reaches the power supply rails. The stated *complexity* invariably refers to the need for additional circuitry to avoid charging of the load capacitor. A popular technique (Comstock, 1981; Main et al., 1995), is to simply short circuit the load every 400 ms or so, periodically discharging the load capacitance and returning the DC compliance voltage to ground. This introduces undesirable high-frequency disturbance and severely distorts low-frequency charge signals.

This paper introduces a new type of current and charge amplifier capable of providing high accuracy, ultra-low frequency regulation of current or charge. The *compliance feedback current or charge amplifier* contains an

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additional output voltage feedback loop that effectively estimates and rejects all sources of DC offset. This technique is intended as a viable alternative for previously presented current and charge amplifiers. In the following sections, a full analysis is provided to clarify the problem and illustrate the simplicity of the solution.

With a view to minimizing structural vibration, the technique of placing an electrical impedance across the terminals of a structurally attached piezoelectric transducer is referred to as piezoelectric shunt damping. One popular technique, resonant shunt damping, is known to provide a significant amount of effective modal damping (Hagood and Von Flotow, 1991; Hollkamp, 1994; Wu and Bicos, 1997; Behrens and Moheimani, 2002). Detrimentally, the circuits may contain a large number of components including impractically large inductors. Although the principal contribution of this paper is to improve the design of current and charge amplifiers for piezoelectric actuation, the last section is dedicated more specifically to the implementation of resonant piezoelectric shunt damping circuits. Other shunting techniques include: *switched shunt* or *switched stiffness* techniques (Corr and Clark, 2002), resistive damping (Hagood and Von Flotow, 1991), and active shunts (Behrens et al., 2003).

Since its introduction, the synthetic impedance (Fleming et al., 2000) has allowed the simplified implementation of piezoelectric shunt damping circuits. The arbitrary nature of the implemented admittance has also permitted the development of new shunt impedances not corresponding directly to a physical circuit (Moheimani et al., 2001; Fleming and Moheimani, 2002). In "Implementation of Admittance/Impedance Transfer Functions," a set of block diagram transformations are presented that link the topology of admittance transfer function block diagrams to shunt circuit schematics. This section is intended for both: practitioners, to simplify the design of analog and digital signal filters, and for researchers, as a new technique for electrical network synthesis. In "Experimental Application" the presented current source and circuit transformations are applied to shunt damp 4 modes of a simply supported beam.

COMPLIANCE FEEDBACK CURRENT/CHARGE DRIVERS

Consider the simplified diagram of a generic current source (Horowitz and Hill, 1980) shown in Figure 1. The high gain feedback loop and voltage driver works to equate the applied reference voltage v_{ref}, to the sensing voltage v_{s}. In the Laplace domain, at frequencies well within the bandwidth of the control loop, the load current $I_{\text{L}}(s)$ is equal to $V_{\text{ref}}(s)/Z_{\text{s}}(s)$.

If $Z_{\text{s}}(s)$ is a resistor R_{s},

$$I_{\text{L}}(s) = V_{\text{ref}}(s)/R_{\text{s}}. \tag{1}$$

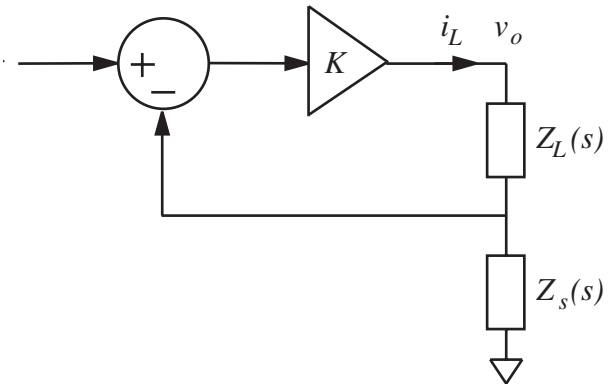

Figure 1. *Generic current source.*

i.e. we have a current amplifier with gain $1/R_{\text{s}}$ A/V.

If $Z_{\text{s}}(s)$ is a capacitor C_{s},

$$\dot{q}_{\text{L}} = I_{\text{L}}(s) = V_{\text{ref}}(s)C_{\text{s}}s, \tag{2}$$

$$q_{\text{L}} = V_{\text{ref}}(s)C_{\text{s}}. \tag{3}$$

i.e. we have a charge amplifier with gain C_{s} Columbs/V.

As mentioned in the introduction, the foremost difficulty in employing such devices to drive highly capacitive loads is that of DC current or charge offsets. Inevitably the voltage measured across the sensing impedance will contain a non-zero voltage offset, this and other sources of voltage or current offset within the circuit result in a net output offset current or charge. As a capacitor integrates DC current, the uncontrolled output voltage will ramp upward and saturate at the power supply rail. Any offset in v_{o} limits the compliance range of the current source and may eventually cause saturation.

To limit the DC impedance of the load, a parallel resistance is often used. With the parallel connection of $1/C_{\text{L}}s$ and R_{L}, the actual current $I_{\text{Lc}}(s)$ flowing through the capacitor is,

$$I_{\text{Lc}}(s) = I_{\text{L}}(s)\frac{s}{s + (1/R_{\text{L}}C_{\text{L}})}. \tag{4}$$

Additional dynamics have been added to the current source, the transfer function now contains a high-pass filter with cutoff $\omega_{\text{c}} = 1/R_{\text{L}}C_{\text{L}}$. That is,

$$\frac{I_{\text{Lc}}(s)}{V_{\text{ref}}(s)} = \frac{1}{R_{\text{s}}}\frac{s}{s + (1/R_{\text{L}}C_{\text{L}})}. \tag{5}$$

In contrast to the infinite DC impedance of a purely capacitive load, the load impedance now flattens out towards DC at $\omega_{\text{c}} = 1/R_{\text{L}}C_{\text{L}}$, and has a DC impedance of R_{L}. A DC offset current of i_{dc} results in a compliance offset of $v_{\text{dc}} = i_{\text{dc}}R_{\text{L}}$. In a typical piezoelectric driving scenario, with $C_{\text{L}} = 100\,\eta F$, and $i_{\text{dc}} = 1\,\mu A$, a $1\,M\Omega$

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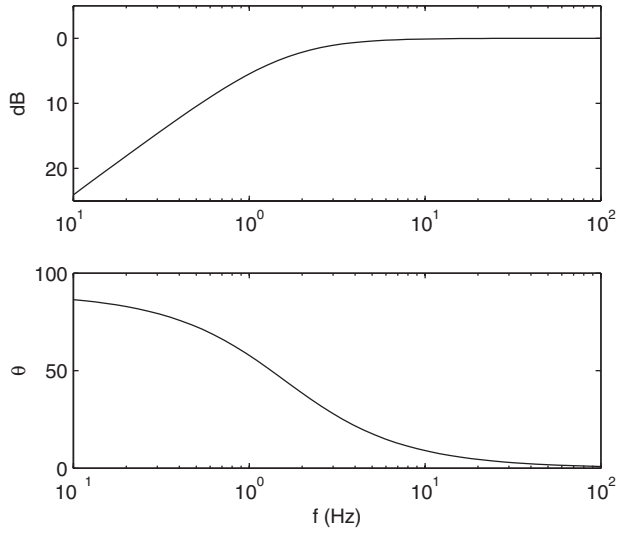

Figure 2. *Typical frequency response from an applied reference voltage to the actual capacitive load current $I_{Lc}(s)$.*

parallel resistance is required to limit the DC compliance offset to 1 V. The frequency response from an applied reference voltage to the actual capacitive load current $I_{Lc}(s)$ is shown in Figure 2. Phase lead exceeds 5° below 18 Hz. Such poor low-frequency response precludes the use of current amplifiers in applications requiring accurate low-frequency tracking, e.g. Atomic Force Microscopy (AFM) (Croft et al., 2000). The advantages of piezoelectric current excitation are lost to the practical electronic difficulties in constructing a current source.

The following section introduces a new type of current source. The *compliance feedback current amplifier* compensates for DC compliance offset without the addition of a parallel resistance. Low-frequency bandwidths in the milli-Hertz range can be achieved with basic components.

Analysis of Compliance Feedback Current and Charge Amplifiers

The aim of this subsection is to introduce a generalized compliance feedback current or charge amplifier. From the general description of its operation, a class of controllers is introduced that achieve excellent ultra-low frequency tracking and complete rejection of DC compliance voltages.

Figure 3 shows the schematic diagram of a compliance feedback current source. Neglecting the input associated with the compliance controller $C(s)$, the circuit is simply a realization of the simplified diagram in Figure 1. The inverted[1] reference voltage v_{ref}, is maintained (by the high gain feedback loop) across the sensing impedance $Z_s(s)$. Thus, $I_L(s) = -V_{ref}(s)/Z_s(s)$. The voltage drive circuit, represented by an opamp, is the only required high voltage component $v_o = K(v_+ - v_-)$, where K is the internal open-loop gain.

The additional input v_{bias} in the compliance feedback loop is included to allow for a non-zero compliance reference voltage. When a voltage is applied to v_{bias}, rather than regulating the DC compliance voltage to zero, the DC compliance voltage is regulated to v_{bias}. In cases where the operational voltage range of the piezoelectric transducer is non-symmetric, for example, a stack actuator, the application of a DC bias voltage electrically pre-stresses the actuator to allow bi-polar operation. Because we are now controlling both the current and voltage in different frequency regions, dynamic bi-polar charge and current signals can be tracked together with a desired DC electrical pre-stressing voltage. For purely capacitive loads, DC electrical pre-stressing requires no additional power.

For high power, or ultra-efficient current and charge amplifiers, the output driver stage can be replaced with a pulse width modulated DC–AC inverter (Mohan et al., 1995; Chandrasekaran et al., 2000). The time delay inherent in switching amplifiers, now enclosed in the current or charge feedback loop will limit the high frequency bandwidth of the amplifier. Aside from the addition of switching noise and current ripple, the following linear results also apply.

The voltages and currents of interest are related in the system block diagram shown in Figure 4. The auxiliary signal v_p models a load internal voltage source, e.g. the piezoelectric voltage. By definition, the polarity of the source hinders the current i_L.

To control the amplifier, there are two objectives. The first is to ensure good reference tracking of the current or charge signals. The second is to provide low frequency and DC regulation of the compliance voltage v_o. Obviously both goals cannot be achieved independently. To understand the trade-off between tracking performance and compliance regulation, two transfer functions are studied: (1) the transfer function from an applied reference voltage $V_{ref}(s)$ to the voltage measured across the sensing impedance $V_s(s)$, and (2) the transfer function from an applied reference voltage $V_{ref}(s)$ to the compliance voltage $V_o(s)$. Respectively, the first transfer function represents the tracking performance, while the second represents the charge or current offset rejection. As the most significant source of output voltage offset is usually DC error in the reference signal, input charge and current offset rejection is studied as opposed to an output disturbance.

In some circumstances, for example, scanning applications where absolute tracking accuracy is required for a short time, it may be beneficial to temporarily hold the output of the compliance controller static. During this time, the charge and current tracking will be perfect but

[1]The inversion of v_{ref} is performed purely for convenience when implementing shunt damping circuits. For this application, the current is usually defined flowing *into* the current source.

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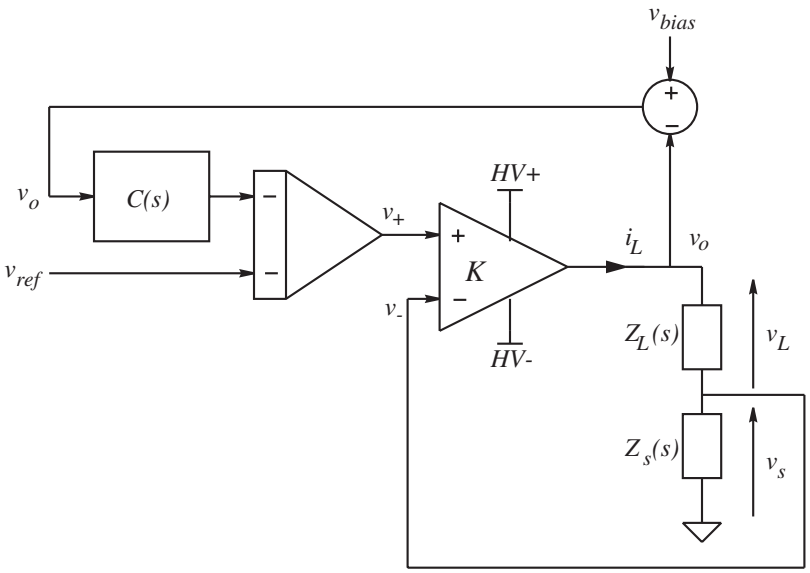

Figure 3. *Simplified schematic of a compliance feedback current amplifier.*

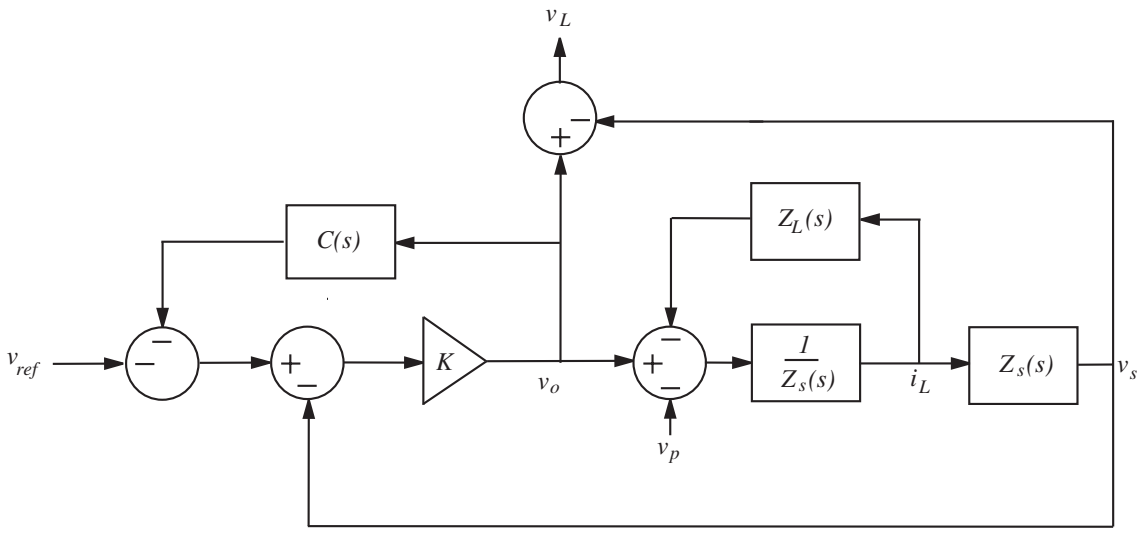

Figure 4. *System block diagram of the circuit shown in Figure 3.*

the output voltage may drift from the reference point. To re-tune the circuit between scans, the compliance controller is simply re-activated and allowed to settle.

For a current source connected to a capacitive load, $Z_s(s) = R_s$ and $Z_L(s) = 1/C_L s$, assuming $V_p(s) = 0$,

$$\frac{V_s(s)}{V_{ref}(s)} = \frac{-KR_sC_Ls}{(1 + KC(s))(R_sC_Ls + 1) + KR_sC_Ls} \quad (6)$$

$$\frac{V_o(s)}{V_{ref}(s)} = \frac{-KR_sC_Ls - K}{(1 + KC(s))(R_sC_Ls + 1) + KR_sC_Ls}. \quad (7)$$

The effect of three compliance controllers is discussed below. Figures 5–7 compare the responses of each control strategy, proportional, integral, and PI. To be fair, numerical values are selected so that each strategy has a comparable low-frequency tracking performance.

(a) Our first choice of controller is simply a proportional controller $C(s) = c$. The effect on the transfer functions $V_s(s)/V_{ref}(s)$ and $V_o(s)/V_{ref}(s)$ is shown in Figures 5(a) and 6(a). The transient response of the compliance voltage to a step in DC offset current is shown in Figure 7(a). Analogous to the effect of adding a parallel resistor, the transfer function $V_o(s)/V_{ref}(s)$ *flattens out* towards DC limiting the integration of offset currents. As shown in Figure 7(a), any offset current results in a large compliance offset. Beneficially the voltage across the sensing resistance is still proportional to the load current, i.e. even though the dynamic response is no better than when a simple resistor is connected across

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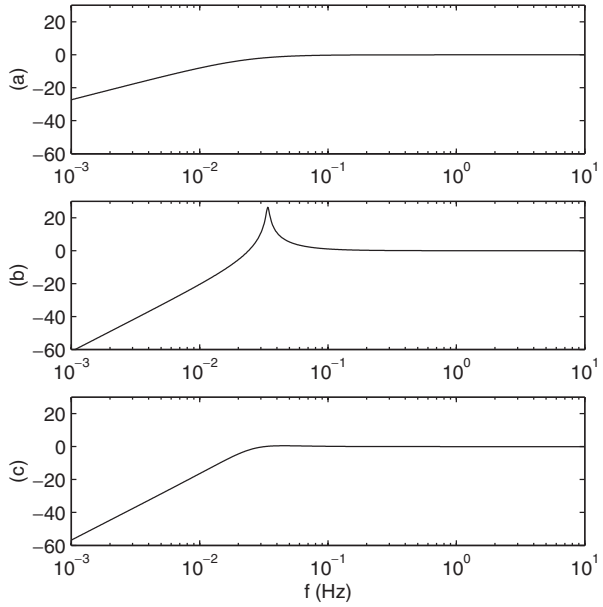

Figure 5. *The current tracking performance $V_s(s)/V_{ref}(s)$ of a current source with capacitive load and compliance controller: (a) Proportional; (b) integral; (c)PI.*

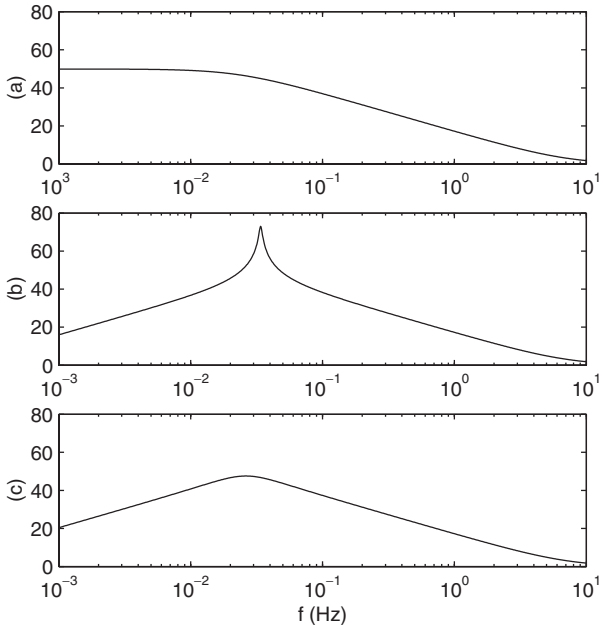

Figure 6. *The compliance regulation performance $V_o(s)/V_{ref}(s)$ of a current source with capacitive load and compliance controller: (a) Proportional; (b) integral; (c) PI.*

the load, we are now able to measure the load current outside the low-frequency bandwidth of the amplifier.

(b) To eliminate DC compliance offset, the next obvious choice is integral control $C(s) = \alpha/s$. Referring to Figures 5, 6 and 7(b) the DC compliance offset is completely rejected but a lightly damped low-frequency resonance has been introduced. As demonstrated in Figure 7(b), the result is an extremely poor settling time.

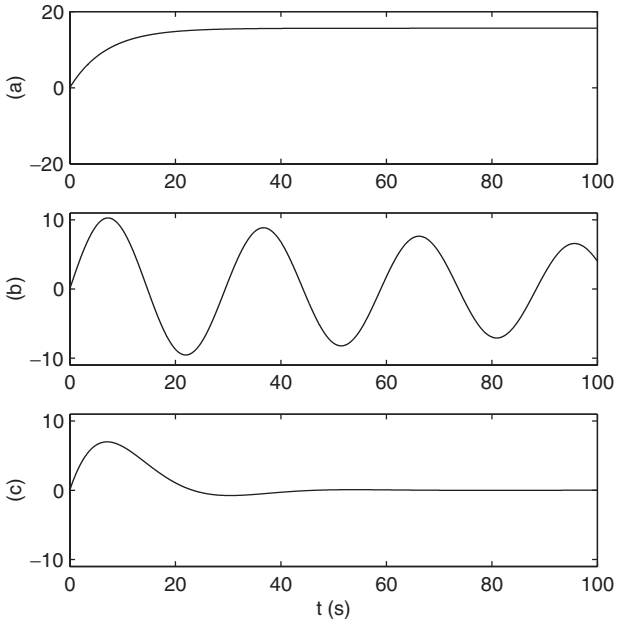

Figure 7. *The transient response of the compliance voltage $V_s(s)$ to a step in DC offset current: (a) Proportional; (b) Integral; (c) PI.*

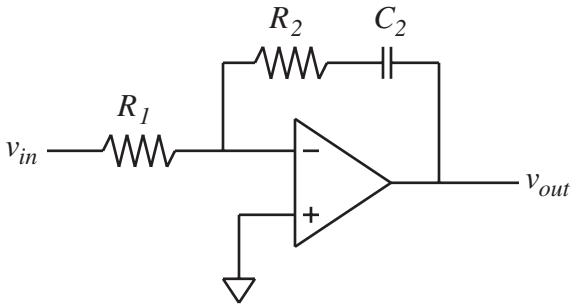

Figure 8. *Opamp implementation of an inverting PI controller.*

(c) Proportional-integral (PI) control $C(s) = \alpha s + \delta/s$ achieves complete rejection of offset currents while exhibiting a fast settling time in the transient response. Using the variables α, δ, and R_s, an arbitrary low-frequency bandwidth can be obtained with full control over the system damping. Figures 5, 6 and 7(c) show superior performance in all of the qualifying responses. A PI controller is easily implemented using the simple opamp circuit shown in Figure 8. The corresponding transfer function is,

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{1/C_2R_1 + (R_2/R_1)s}{s} \tag{8}$$

For a charge amplifier connected to a capacitive load, $Z_s(s) = 1/C_s s$ and $Z_L(s) = 1/C_L s$, we may write,

$$\frac{V_s(s)}{V_{\text{ref}}(s)} = \frac{-KC_L}{(1 + KC(s))(C_L + C_s) + KC_L} \tag{9}$$

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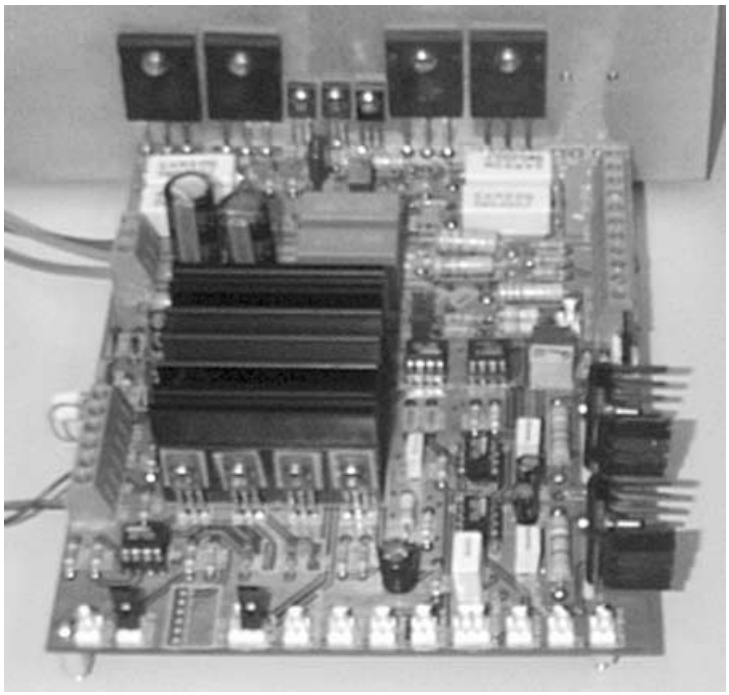

Figure 9. *Photograph of a prototype current/charge amplifier.*

$$\frac{V_o(s)}{V_{ref}(s)} = \frac{-KC_L - KC_s}{(1 + KC(s))(C_L + C_s) + KC_L} \tag{10}$$

The compliance controller design for charge amplifiers is considerably easier. Simple integral control ($C(s) = \alpha/s$) results in a first-order response with complete regulation of DC offsets.

$$\frac{V_o(s)}{V_{ref}(s)} = \frac{-KC_L s - KC_s s}{(KC_L + C_L + C_s)s + K\alpha(C_L + C_s)} \tag{11}$$

The location of the closed loop pole is easily manipulated by the variable α.

Note that charge amplifiers are actually susceptible to DC offsets in two of the circuit node-voltages: (1) the output compliance voltage v_o, and (2) the sensing voltage v_s. Offset in the sensing voltage results from input bias currents generated by the driving opamp. By choosing an opamp with low input bias current, for example an opamp with JFET input transistors[2], the problem can be solved by placing a large shunt resistor in parallel. Although this introduces additional dynamics, the low-frequency cutoff in the sensing voltage measurement would typically be two orders of magnitude lower than that of the compliance regulation loop. The additional dynamics can be safely neglected.

[2]Junction Field Effect Transistors (JFETs) are commonly used in the input stages of high voltage opamps.

If operation below 0.1 Hz is required, the initial settling time of the compliance controller will become significant. This can be avoided if a small logic circuit is included to decrease the settling time (by increasing α) for a short time during initialization.

Experimental Results

In this section, experimental results are presented for a prototype current and charge amplifier shown in Figure 9. Features include:

- Maximum supply voltage of +/−250 V.
- Peak output current of 32 A.
- On-board low-voltage instrumentation supply.
- Reconfigurable to drive current, charge, voltage or current rate-of-change.
- Variable bandwidth up to 150 kHz (100 nF PZT load).
- Highly linear and low-cost discrete BJT components.
- Fully protected high bandwidth ultra-high impedance instrumentation of the terminal voltage, compliance voltage, current, charge, and current rate-of-change.
- Capable of accepting impedance cards (as discussed in "Analog Synthesis").

To illustrate the operation of the current amplifier, a 1 μF capacitor is driven at low frequencies with a current sensing resistor of 220 kΩ. With $C(s) = 0.004s + 0.00016/s$, the simulated compliance and tracking frequency responses are shown in Figures 10 and 11.

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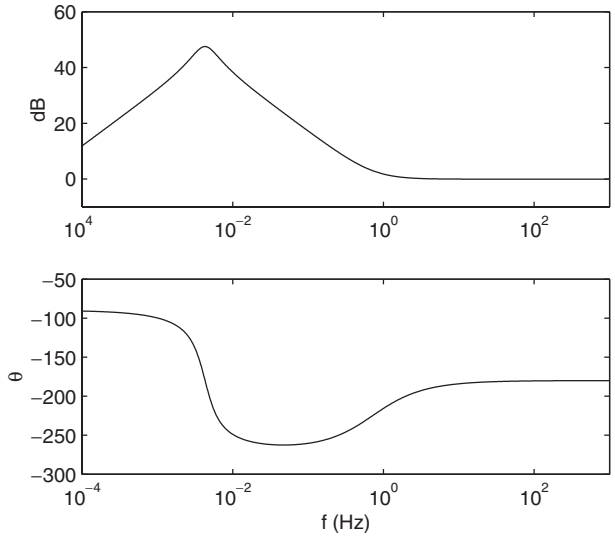

Figure 10. *Simulated compliance frequency response $V_o(s)/V_{ref}(s)$ of the prototype current source.*

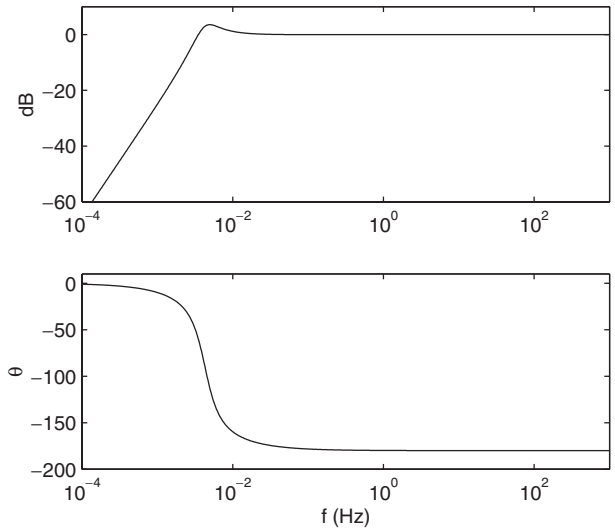

Figure 11. *Simulated tracking frequency response $V_s(s)/V_{ref}(s)$ of the prototype current source.*

The transient response to a step change in input current reference offset is shown in Figure 13. A 100 mHz signal is applied to examine the low-frequency tracking performance, the reference and measured currents are shown in Figure 12.

Similar experiments were carried out for a charge amplifier. Using a sensor capacitance of 10 μF, the compliance controller $C(s) = 0.001/s$ provides the desired response. Analogous frequency and time domain results are presented in Figures 14–17.

IMPLEMENTATION OF ADMITTANCE/ IMPEDANCE TRANSFER FUNCTIONS

Referring to Figure 18, the terminal impedance of an arbitrary electrical network $Z_T(s)$ can be implemented

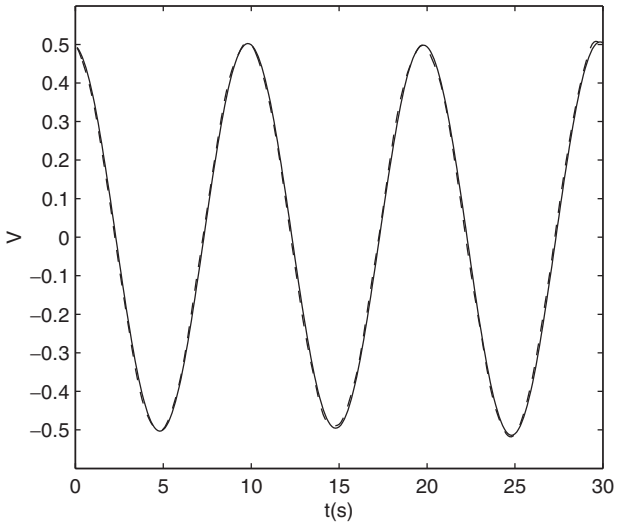

Figure 12. *Reference (–) and measured current (----).*

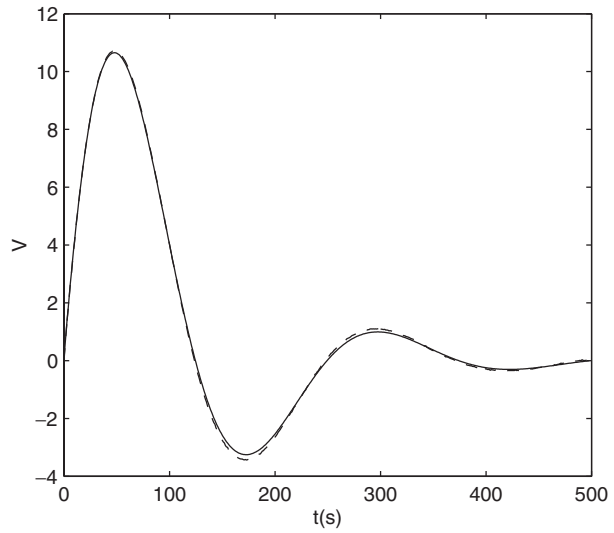

Figure 13. *Simulated (–) and measured (----) compliance response to a step change in current offset.*

by either: (a) measuring the terminal current i_z and controlling the terminal voltage v_z, or (b) measuring the terminal voltage v_z and controlling the terminal current i_z. The motivation and benefits behind such techniques are thoroughly discussed in (Fleming et al., 2000, 2002).

For the first case in Figure 18(a), the controlled voltage v_z is set to be a function of the measured current i_z. i.e. $v_z = f(i_z)$. If the function $f(i_z)$, is a linear transfer function $Z(s)$ whose input is the measured current i_z, i.e. $V_z(s) = Z(s)I_z(s)$, then the terminal impedance $Z_T(s)$ is equal to $Z(s)$.

Similarly for the second case, Figure 8(b), the controlled current i_z is set to be a function of the measured voltage v_z, i.e. $i_z = f(v_z)$. If the function $f(v_z)$, is a linear transfer function $Y(s)$ whose input is the measured voltage, i.e. $I_z(s) = Y(s)V_z(s)$, then the terminal admittance $Y_T(s)$ is equal to $Y(s)$.

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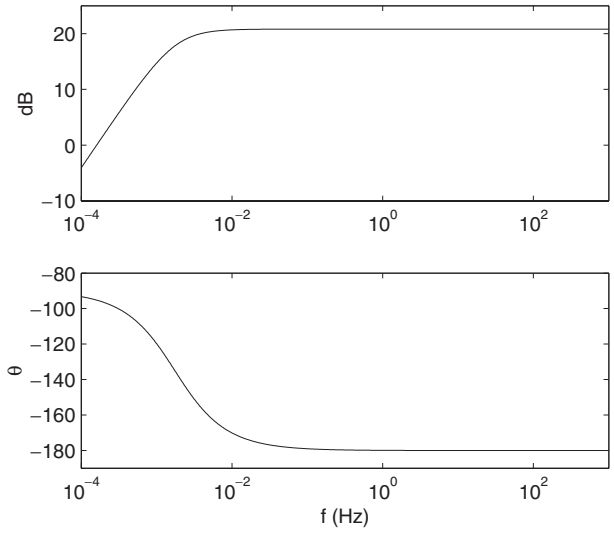

Figure 14. *Simulated compliance frequency response $V_o(s)/V_{ref}(s)$ of the prototype charge amplifier.*

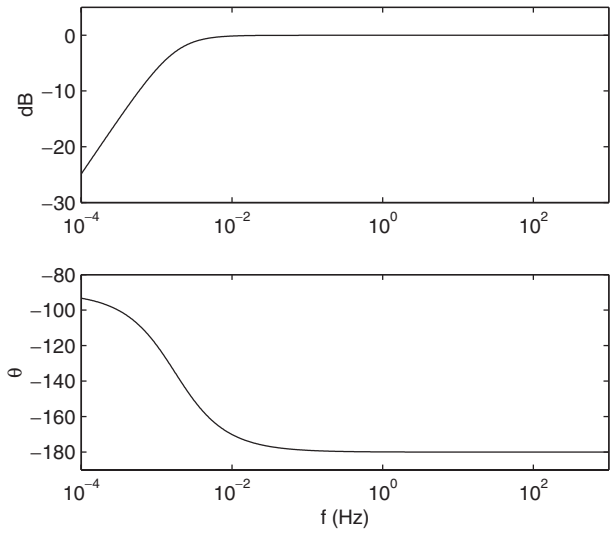

Figure 15. *Simulated tracking response $V_s(s)/V_{ref}(s)$ of the prototype charge amplifier.*

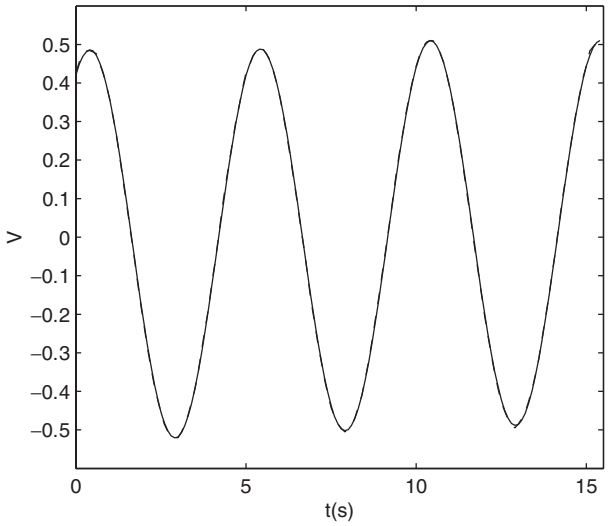

Figure 16. *Reference (–) and measured charge (- -)*

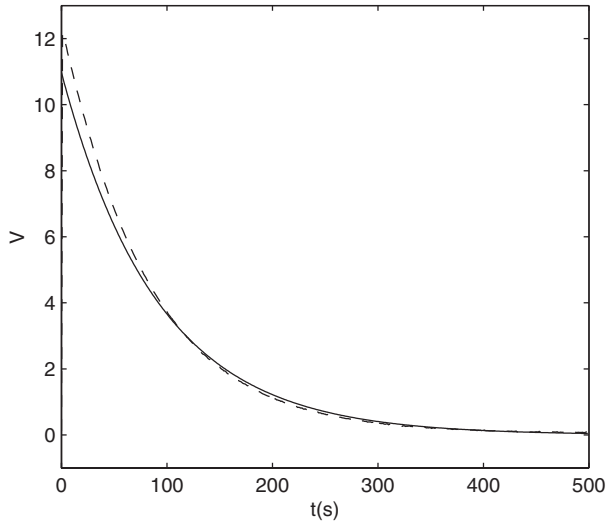

Figure 17. *Simulated (–) and measured (- -) compliance response to a step change in reference offset.*

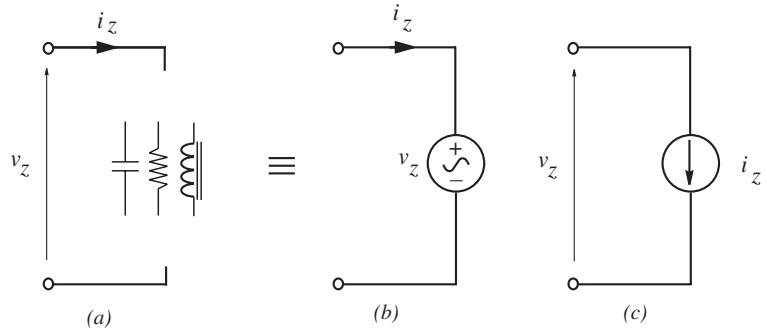

Figure 18. *An arbitrary terminal impedance (a), a synthetic impedance (b), and a synthetic admittance (c).*

The choice of configuration, either synthetic impedance or synthetic admittance, will depend on the relative order of the desired impedance. As implementation of improper transfer functions (Kailath, 1980) is impractical, the choice should be made so that the required transfer function $Z(s)$ or $Y(s)$ is at least proper (Kailath, 1980). Examples of admittance implementation can be found in (Fleming et al., 2000a,b, 2002;

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Moheimani et al., 2001, 2002; Behrens and Moheimani, 2002; Fleming and Moheimani, 2002).

Block Diagram Transformations

As discussed above, to synthesize an electrical network, a filter is required with the same transfer function as the impedance or admittance of that circuit. When using a DSP system, the filter can be implemented simply by calculating the electrical impedance and implementing that transfer function directly. The task may become tedious or complicated if the electrical circuit contains a large number of components. A 'current blocking' piezoelectric shunt circuit (Wu, 1999) may contain up to 18 individual components in a 3-mode circuit. The admittance transfer function would contain 15 states and be parameterized in up to 18 variables.

Analog implementation adds further difficulty. Traditional filter synthesis techniques (Van Valkenburg, 1982) typically require a partial fraction decomposition, followed by the implementation of each second-order section.

Neither direct analog nor digital implementation is particularly straight-forward for complicated impedance structures. For second-order transfer functions and above, the resulting digital or analog filter can be difficult to tune.

To simplify the process of impedance or admittance transfer function implementation, this section introduces a link between the topology of system block diagrams and circuit schematics. In the digital case, if a graphical compilation package such as the real time workshop for Matlab or similar is available, no impedance calculation from the circuit diagram is required at all. The resulting block diagram bears a natural resemblance to its corresponding circuit, is clearly parameterized, and is consequently easy to tune. In the analog case, the circuit can be broken down into a number of simple opamp integrators and amplifiers whose gains correspond directly to component values. The resulting filter circuit is practical, easy to implement, expandable, and simple to tune.

Following are the transformations of interest for both impedance and admittance synthesis cases. In "Examples", two examples are presented to clarify the application.

IMPEDANCE SYNTHESIS

Parallel equivalence Consider the parallel network components $Z_1, Z_2, \ldots, Z_m$ as shown in Figure 19. The terminal impedance and admittance corresponding to this network is:

$$Z_T(s) = \frac{1}{(1/Z_1) + (1/Z_2) + \cdots + (1/Z_m)}$$
$$Y_T(s) = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_m} \tag{12}$$

Now consider the transfer function block diagram, also shown in Figure 19

$$G(s) = \frac{T(s)}{R(s)} = \frac{Z_1}{1 + Z_1(1/Z_2) + \cdots + Z_1(1/Z_m)} = \frac{1}{(1/Z_1) + (1/Z_2) + \cdots + (1/Z_m)} \tag{13}$$

Observe that $Y_T(s)$ and $G(s)$ as described in Equations (12) and (13) are identical. Therefore, if a synthetic impedance as shown in Figure 18(b) is implemented with a transfer function equal to $G(s)$, the impedance seen from the terminals is identical to the impedance of the parallel network shown in Figure 19 (with impedance $Z_T(s)$ given by (12)).

Series equivalence Consider the series network components $Z_1, Z_2, \ldots, Z_m$ as shown in Figure 20. The terminal impedance and admittance of this network are:

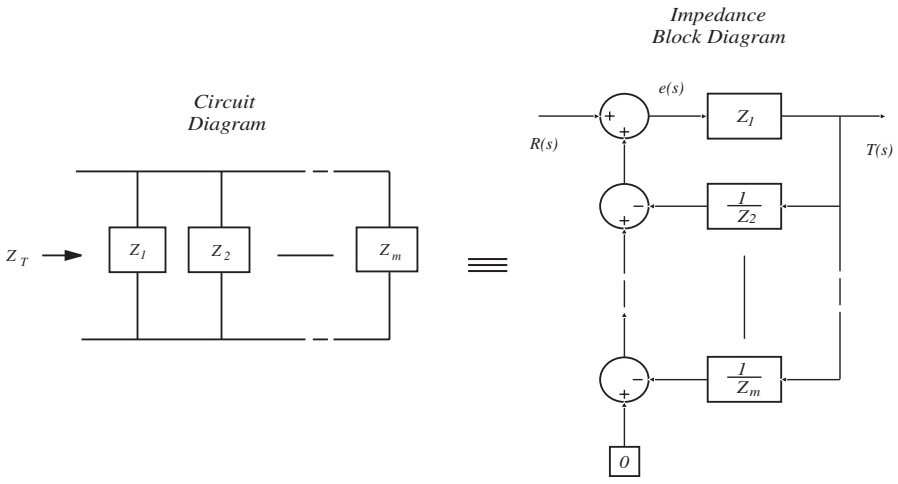

Figure 19. *Parallel equivalence for impedance block diagrams.*

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$$Z_T(s) = Z_1 + Z_2 + \cdots + Z_m$$
$$Y_T(s) = \frac{1}{Z_1 + Z_2 + \cdots + Z_m} \tag{14}$$

Now consider the transfer function block diagram, also shown in Figure 20

$$G(s) = \frac{T(s)}{R(s)} = Z_1 + Z_2 + \cdots + Z_m \tag{15}$$

Observe that $Y_T(s)$ and $G(s)$ as described in Equations (14) and (15) are identical. Therefore, if a synthetic impedance as shown in Figure 18(b) is implemented with a transfer function equal to $G(s)$, the impedance seen from the terminals will be identical to the impedance of the series network shown in Figure 20 (with impedance $Z_T(s)$ given by (14)).

ADMITTANCE SYNTHESIS

Parallel equivalence Consider the parallel network components $Z_1, Z_2, \ldots, Z_m$ as shown in Figure 21. The terminal impedance and admittance of this network is

$$Z_T(s) = \left(\frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_m}\right)^{-1}$$
$$Y_T(s) = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_m} \tag{16}$$

Now consider the transfer function block diagram, also shown in Figure 21.

$$G(s) = \frac{T(s)}{R(s)} = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_m} \tag{17}$$

Observe that $Y_T(s)$ and $G(s)$, as described in Equations (16) and (17) are identical. Therefore, if a synthetic impedance as shown in Figure 18(b) is implemented with a transfer function equal to $G(s)$, the impedance seen from the terminals is identical to the impedance of the parallel network shown in Figure 21 (with impedance $Z_T(s)$ given by (16)).

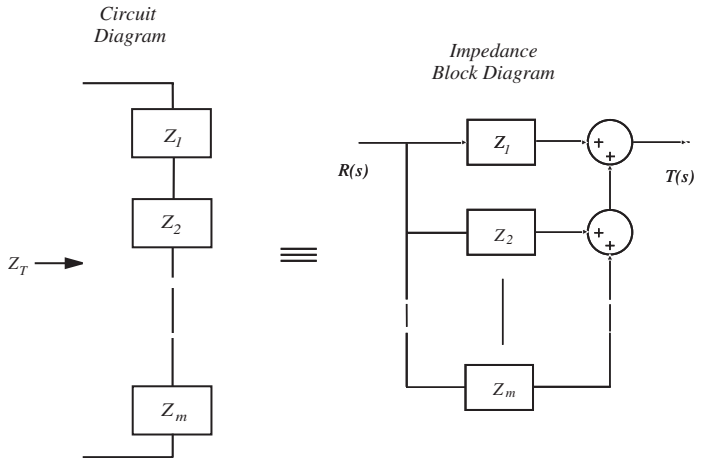

Figure 20. *Series equivalence for impedance block diagrams.*

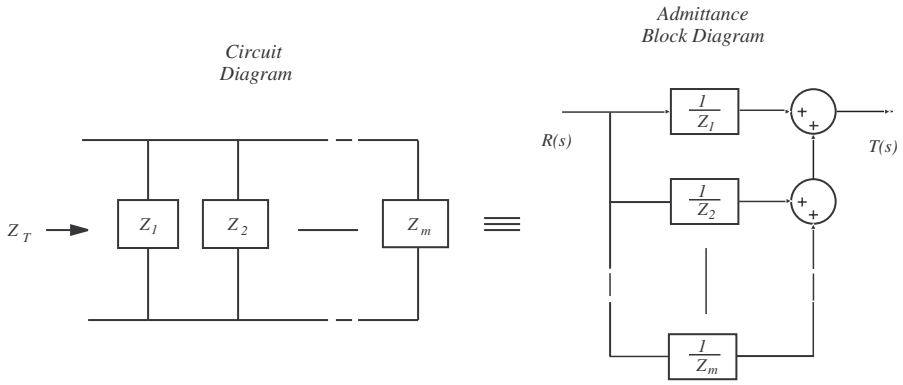

Figure 21. *Parallel equivalence for admittance block diagrams.*

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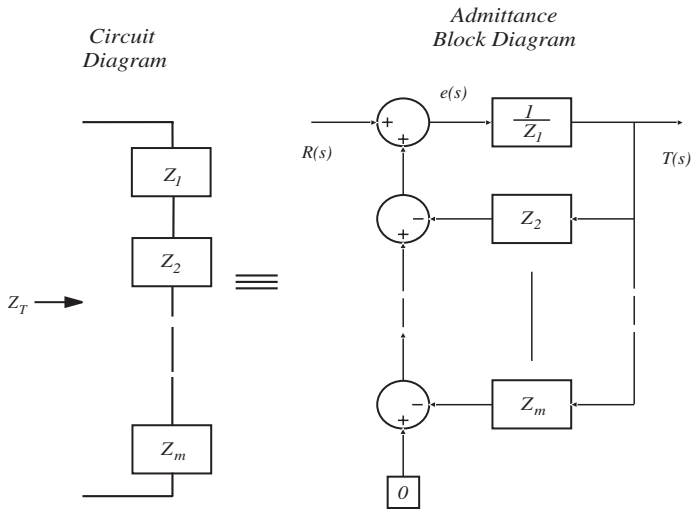

Figure 22. *Series equivalence for admittance block diagrams.*

Series equivalence Consider the series network components $Z_1, Z_2, \ldots, Z_m$ as shown in Figure 22. The terminal impedance and admittance of this network is:

$$\begin{aligned} Z_{\mathrm{T}}(s) &= Z_1 + Z_2 + \cdots + Z_m \\ Y_{\mathrm{T}}(s) &= \frac{1}{Z_1 + Z_2 + \cdots + Z_m} \end{aligned} \tag{18}$$

Now consider the transfer function block diagram, also shown in Figure 22

$$\begin{aligned} G(s) = \frac{T(s)}{R(s)} &= \frac{1/Z_1}{1 + (1/Z_1)Z_2 + \cdots + (1/Z_1)Z_m} \\ &= \frac{1}{Z_1 + Z_2 + \cdots + Z_m} \end{aligned} \tag{19}$$

Observe that $Y_{\mathrm{T}}(s)$ and $G(s)$ as described in Equations (18) and (19) are identical. Therefore, if a synthetic impedance as shown in Figure 18(c) is implemented with a transfer function equal to $G(s)$, the impedance seen from the terminals is identical to the impedance of the series network shown in Figure 22 (with impedance $Z_{\mathrm{T}}(s)$ given by (18)).

Examples

DIGITAL SYNTHESIS

Consider the current blocking circuit (Wu, 1999) shown in Figure 23. The corresponding admittance block diagram is shown in Figure 24. Each subsystem can be further decomposed or implemented by parameterized state space system. Both methods facilitate simplified online tuning.

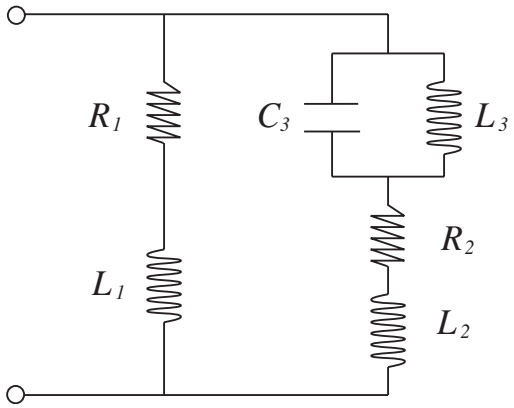

Figure 23. *Current blocking shunt circuit.*

ANALOG SYNTHESIS

Current flowing shunt circuits have recently been introduced (Behrens and Moheimani, 2002). The shunt circuit is simple and increases in order only linearly as the number of modes to be shunt damped simultaneously increases[3]. Combined with the simple tuning procedure, current flowing shunt circuits extend gracefully to applications involving a large number of high profile modes, e.g. a simply supported plate, where 5 modes are damped simultaneously (Behrens et al., 2002).

To implement the admittance of a current flowing shunt circuit, a filter that represents a single circuit branch is required. The output of each branch filter can then be summed to produce a filter representing the entire multimode circuit.

To implement the admittance of a single branch, one may first consider the traditional filter synthesis techniques of state-variable or Sallen-Key (Van Valkenburg,

[3]In contrast to current blocking techniques that increase in order quadratically.

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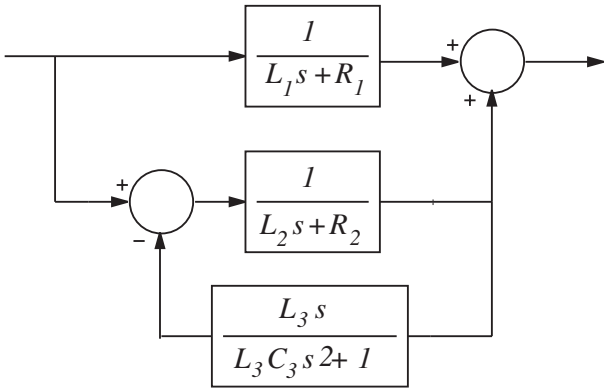

Figure 24. *Admittance transfer function block diagram of a current flowing shunt circuit.*

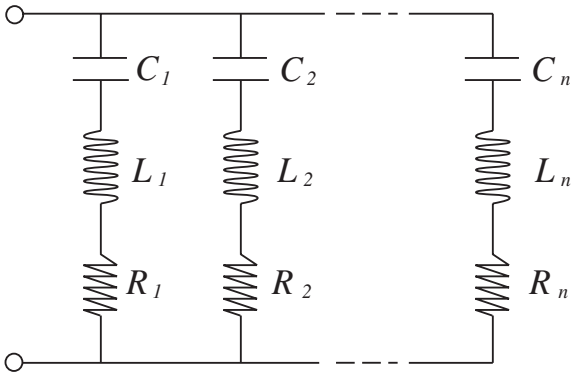

Figure 25. *Current flowing shunt circuit.*

1982). Such techniques result in a circuit whose component values are a complicated function of the original shunt components, severely impeding any attempt at online tuning. Alternatively, using the transformations presented in this section, each admittance branch can be implemented first as a system block diagram, then as an analog circuit containing only summers, integrators, and gains.

The admittance block diagram of a single mode current flowing shunt circuit is shown in Figure 26. A simple but effective analog implementation is shown in Figure 27. The transfer function is easily found to be,

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{1}{R_1 C_1 s + R_2/R_3 + (1/R_4 C_4 s)}. \qquad (20)$$

The filter components are related to the original shunt circuit branch by,

$$\begin{aligned} L &= R_1 C_1 \\ R &= R_2/R_3 \\ C &= R_4 C_4. \end{aligned} \qquad (21)$$

Although there are more opamps than would normally be required, the transfer function is explicitly parameterized in terms of the parent circuit. The resistors R_1, R_2, and R_4 can be varied independently to tune the shunt circuit inductance, resistance, and capacitance.

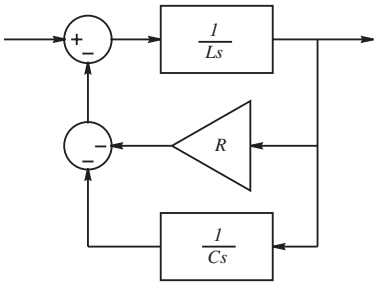

Figure 26. *A single current flowing branch admittance block diagram.*

A practical implementation is shown in Figure 28. For flexibility, the filter is manufactured as a small board that can be installed or removed as necessary. The pictured current source has a maximum supply voltage of ±45 V, includes an on-board low voltage supply, and can hold up to two impedance cards.

The high voltage amplifier presented in "Experimental Results" is also capable of accepting impedance cards. This technology represents a considerable increase in the practicality and simplicity of piezoelectric shunt damping systems.

EXPERIMENTAL APPLICATION

In this section, a synthetic admittance is employed, implementing a current-flowing shunt circuit (Behrens and Moheimani, 2002) (shown in Figure 25), to damp 4 modes of a simply supported beam. The experimental piezoelectric laminate beam is shown in Figure 29. The dimensions and physical parameters of the beam and piezoelectric transducers can be found in (Behrans and Moheimani, 2002).

In this experiment, one of the piezoelectric transducers is shunted with an electrical impedance to minimize the vibration resulting from a disturbance applied to a second co-located piezoelectric patch. The complete shunt circuit design process and resulting component values can be found in (Behrans and Moheimani, 2002).

As discussed in "Examples", an equivalent Simulink block diagram is generated with an identical admittance transfer function to that of the ideal circuit. The Real Time Workshop for Matlab is then invoked to generate the required C code, compile it, then download the resulting program to a dSpace DS1103 rapid prototyping system. By altering the subsystem gains online, the shunt circuit is finely tuned to the structural resonance frequencies.

The experimental open loop and shunt damped frequency responses from an applied actuator voltage

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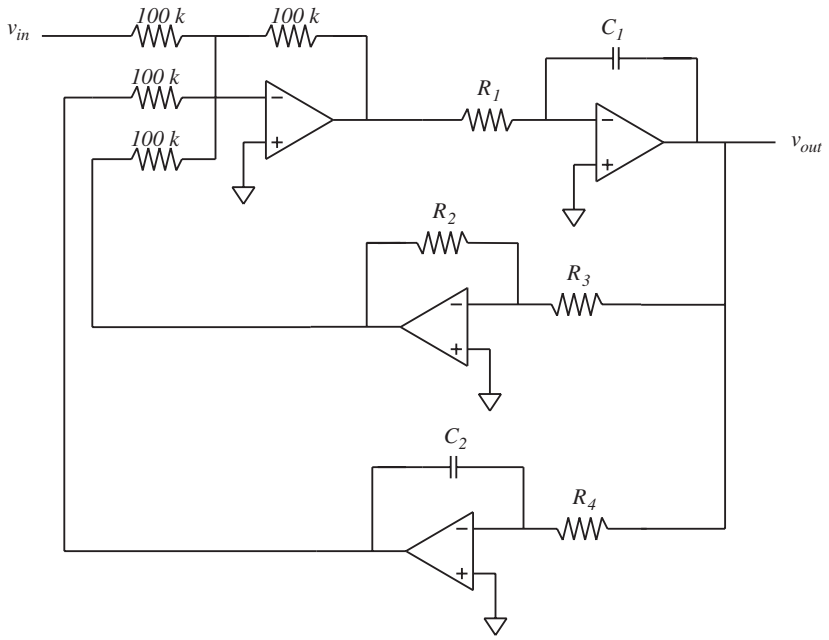

Figure 27. *Analog implementation of the block diagram shown in Figure 26.*

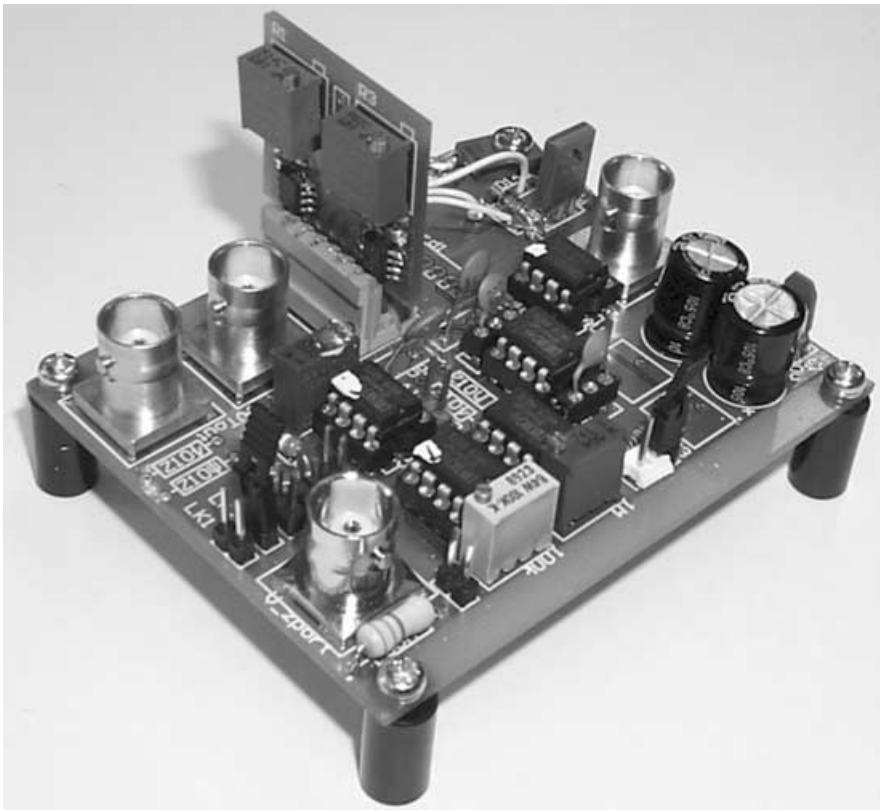

Figure 28. *An opamp-based current source with impedance card mounted vertically.*

to the resulting displacement at a point are shown in Figure 30. It can be observed that a significant amount of modal damping has been added to the structure.

5 CONCLUSIONS

A new class of current and charge amplifiers have been introduced. By feeding back the amplifier's compliance

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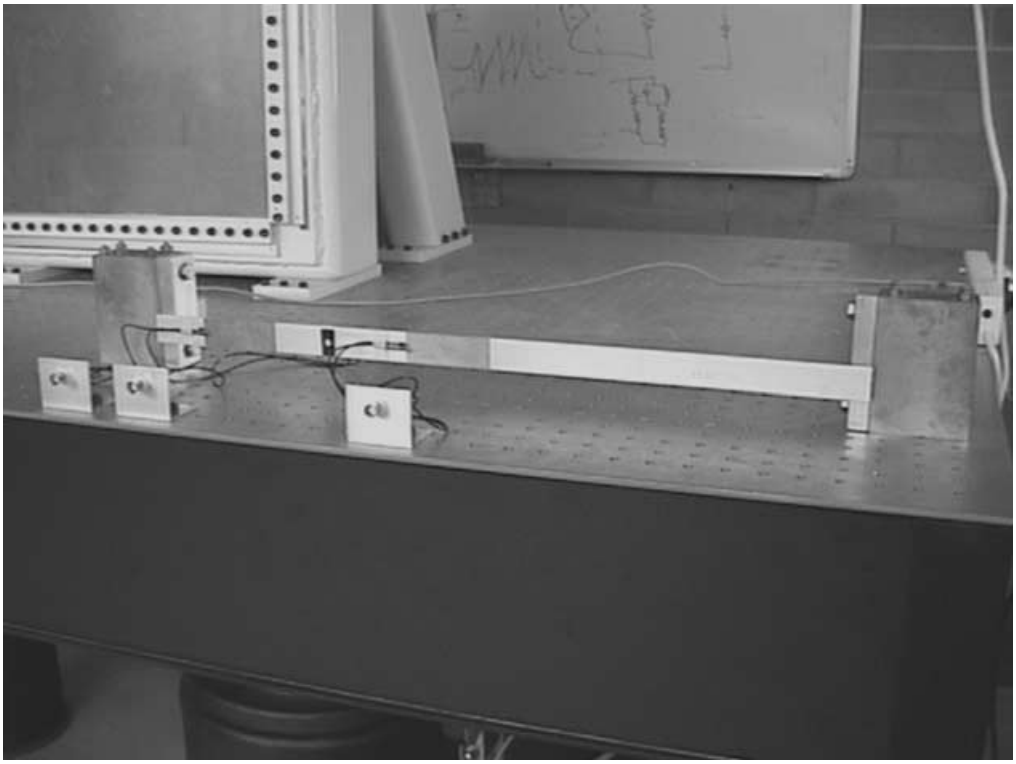

Figure 29. *Experimental beam.*

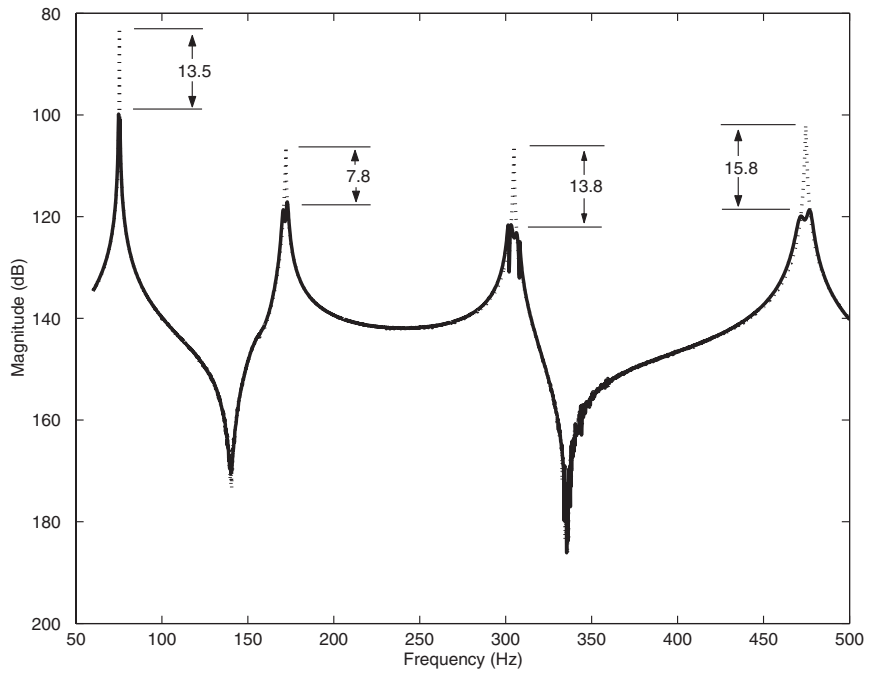

Figure 30. *Experimental open loop (···) and shunt damped (–) magnitude transfer function from an applied actuator voltage to the resulting displacement.*

voltage, the effect of DC circuit offsets can be eliminated. Experimental results show excellent low-frequency current and charge tracking and complete rejection of DC offsets. A prototype compliance feedback amplifier connected to a purely capacitive load is shown to accurately realize low-frequency current and charge signals.

One application of piezoelectric current sources is in the field of shunt damping, i.e. the reduction of structural

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vibration with the use of an attached piezoelectric transducer and electrical impedance. To avoid implementing impractically large inductors or nonideal virtual circuits, the synthetic admittance can be employed to implement an ideal electrical network. Block diagram transformations from an arbitrary electrical network have been presented to simplify the realization of the required digital or analog signal filter.

A prototype compliance feedback amplifier connected to a purely capacitive load was shown to accurately realize low-frequency current and charge signals of 100 and 200 mHz respectively.

The prototype current amplifier and the presented block diagram transformations were applied to shunt damp four modes of a simply supported beam.

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