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Highly parallel scanning tunneling microscope based hydrogen depassivation lithography

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Hydrogen depassivation lithography (HDL) carried out by a scanning tunneling microscope has sub-nm resolution and the potential to create atomically precise patterns. However, as a serial write tool, it is subject to Tennant's law which fairly accurately predicts an extremely low areal throughput in line with their experimental results. In order to improve the throughput, the authors explore the feasibility of an approach to develop a highly parallel exposure system, which preserves the ability to perform truly atomically precise patterning. The obvious way to increase scanning probe lithography throughput is to increase the number of probes. In this paper, they compare existing multiple scanning probe systems [D. S. Ginger, H. Zhang, and C. A. Mirkin, Angew. Chem. Int. Ed. **43**, 30 (2004) and P. Vettiger *et al.*, Microelectronic **46**, 11 (1999)] with their proposed highly parallel, MEMS-based scanners with three degrees of freedom (3 DoF) movement. Additionally, since HDL is a version of e-beam lithography, they examine the problems encountered by the attempts to go parallel with conventional e-beam lithography and why highly parallel HDL avoids these physical and engineering problems. While there are still some engineering challenges to be met, the path to massively parallel HDL tip arrays is relatively straightforward. They believe that 3 DoF MEMS-based independently controlled scanners could be placed with a density of 10 100/cm^2. That density range implies 7×10^6 tips on a 300 mm wafer. However, they do want to make clear that they do not contend that even this level of parallelism will make HDL a contender for producing CMOS consumer electronics. *Published by the AVS.*
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I. INTRODUCTION

While the atomic precision capabilities of HDL make it an attractive candidate for a number of exciting applications such as quantum computing[1] and quantum meta materials,[2] as predicted by Tennant's law,[3,4] a serial write tool with 0.768 nm resolution has an extremely limited throughput. This will relegate HDL with a single tip to research applications and most likely will preclude scalable manufacturing.

In this paper, we explore the feasibility of a path to HDL which could achieve manufacturing throughput by achieving highly parallel operation of tips that have independent X, Y, and Z nanopositioning with excellent precision. It is reasonable to ask if limiting each scanner to independent actuation only in Z is a better approach than independent actuation in XYZ for each scanner since the Z only scanner would be smaller and provide a higher density of operating tips. But the Z only approach imposes limitations that affect patterning efficiencies. With only Z independent actuation for each tip, efficient vector scanning is highly pattern dependent with the worst case being where a large amount of the parallelism is wasted, suggesting that a raster scan approach would be the better approach. However, a raster scan approach, in the general case, requires that the entirety of the scan area be covered by the raster scan, turning the lithography mode on, only when over an area to be exposed. Conventional e-beam lithography has largely abandoned this approach in favor of a vector scan approach which sends the exposure spot on an optimized path to expose only what is required within a scan field. Additionally, the independent three degrees of freedom (3 DoF) are much preferred for HDL because of the requirement to align to the Si surface lattice to within 0.1 nm in order to achieve atomic precision. Even if the discrepancy in the tip position from an ideal grid could be determined (a challenging metrology task), the throughput hit of going to a very tight raster scan (required to take into account the tip position discrepancies) or a time multiplexed vector scan for general patterning capabilities would be very large.

While there are significant engineering problems that will be encountered in scaling to a large number of scanning tunneling microscope (STM) tips operating in parallel and it is instructive to examine the problems encountered by parallel e-beam lithography to see if these can be avoided, we argue that the difficulties in scaling to a much greater level of parallelism will be linear rather than the exponential difficulty of increasing the level of parallelism with conventional e-beam lithography.

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II. HYDROGEN DEPASSIVATION LITHOGRAPHY

HDL is a version of e-beam lithography which uses an STM tip as a cold field emitter to produce a very small beam of low energy electrons to expose a resist which is the limit of a thin self-developing resist, a monolayer of H atoms passivating an Si (100) 2×1 surface.[5,6] HDL is typically carried out in ultrahigh vacuum conditions at room temperature, though operation at cryogenic to ~250 °C is also possible. There are two modes of HDL[7] exposure as depicted in Fig. 1.

In each case, the self-developing exposure mechanism is electron stimulated desorption where electron energy transfer breaks the Si-H bond so that the H desorbs. There is a low-bias (2–5 V) tunneling mode which has sub-nm resolution and is essentially atomic precise (AP). This mode requires a multielectron process for successful exposure which is very inefficient (but enables atomic precision).

We have developed a simple model to better explain why the low-bias exposure mode achieves atomic precision. We start with a simplified expression[8] to calculate the tunnel current between the tip and the sample.

$$i = KVe^{(-2Td\sqrt[2]{2\phi me/\hbar})}, \tag{1}$$

where i = tunneling current, K = constant, V = tip to sample bias, Td = tunnel gap, ϕ = local barrier height (LBH), me = electron mass, and $\hbar$ = Plank's constant/2π.

Using Eq. (1) with $V = 4$ V, $\phi = 4$ eV, and $Td = 1$ nm, we can adjust $K = 0.194$ to produce a tunneling current of 1 nA which is typical of our lithography modes.

Equation (1) with $Td = 1.1$ nm the current is equal to 0.129 nA and Eq. (1) with $Td = 0.9$ nm the current is equal to 7.75 nA. These results produce approximately 1 order of magnitude change in tunneling current with a 0.1 nm change in tip height that is nominally expected with STM operation.

Using Eq. (1) with a simplified physical model allows us to estimate the tunnel current in the vicinity of the tip. Figure 2 shows the simplified model with the Si surface represented as an infinitely flat conducting surface and that all the tunneling current is sourced from a single atom represented by a 0.364 nm sphere or approximately the size of a tungsten atom.

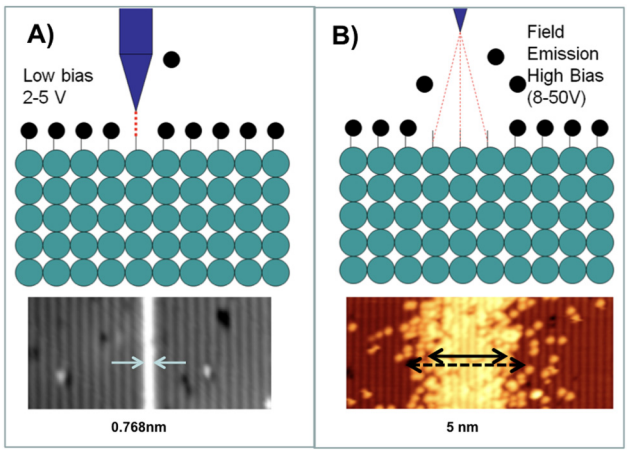


FIG. 1. Two modes of HDL. (a) AP mode, up to about 5 V. (b) Field emission mode, from about 8 V upwards.

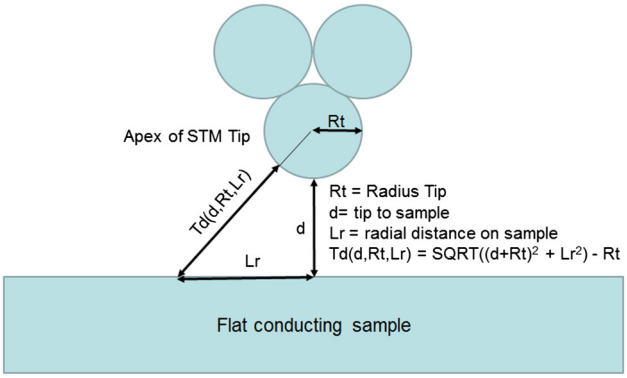


FIG. 2. Simplified physical model for calculating the tunneling current distribution.

Using the model shown in Fig. 2, we can see that the distance from the tip to the sample is a radial distance Lr away from the point on the sample directly under the tip and can be expressed as

$$Td = \sqrt[2]{(d + Rt)^2 + Lr^2} - Rt. \tag{2}$$

Substituting for Td in Eq. (1) produces

$$i(d, Rt, Lr) = KVe^{-2(\sqrt[2]{(d+Rt)^2+Lr^2}-Rt)\sqrt[2]{2\phi me/hbar}}. \tag{3}$$

Equation (3) with $d = 1$ nm and $Rt = 0.162$ nm, as a function of Lr, produces the current distribution shown in Fig. 3.

These calculated data suggest that the current at a lateral distance of 0.5 nm away from the center of the tip drops to roughly 10% of the current directly under the tip. However, the depassivation efficiency, that is the required number or electrons to remove an H atom in the low-bias regime, is a strong function of the current because the low-bias exposure mechanism is a multielectron process. Experimental data from Ref. 9 for different biases and different currents suggest

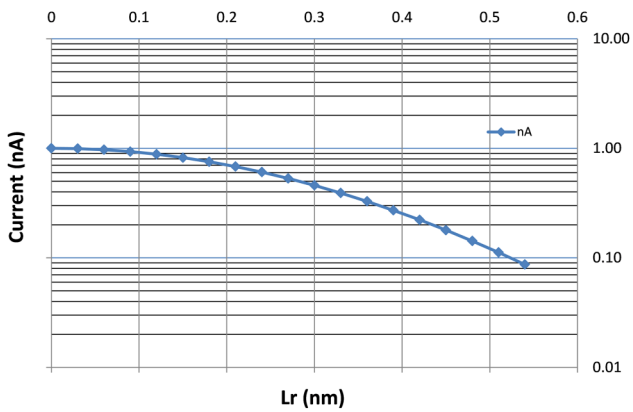


FIG. 3. Calculated STM current distribution on the sample under the tip as a function of radial distance away from a point directly below the tip.

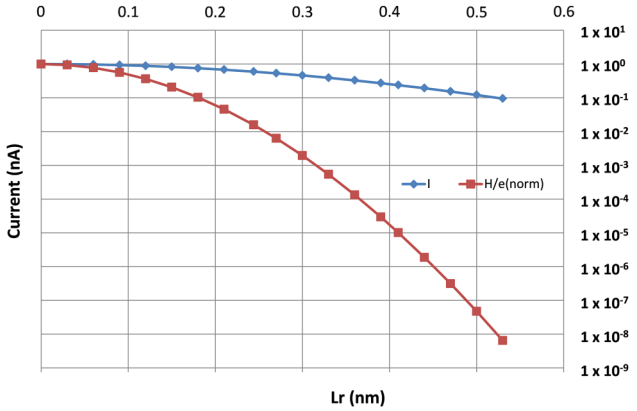


FIG. 4. Calculated current and the normalized depassivation efficiency (H/e) as a function of the radial lateral distance under the tip.

that the depassivation efficiency varies with the eighth power of the current. Taking the eighth power of the current shown in Fig. 3 as the depassivation efficiency demonstrates why HDL has such a high resolution as shown in Fig. 4.

The calculated depassivation efficiency shown in Fig. 4 not only explains the extremely high resolution of the process which allows atomic precision patterning but is also consistant with our experimental lithography data where it is relatively easy to expose H atoms along a dimer row with the tip roughly in the center of the dimer row with H atoms ~0.15 nm on either side of the tip while not exposing H atoms on the adjacent dimer rows (see Fig. 1) which are more than 0.6 nm away and the depassivation efficiency has dropped by more than 8 orders of magnitude.

As the voltage applied to the STM tip increases, fewer electrons are required to remove the H atoms, and the process becomes more efficient. Eventually, depassivation becomes a single-electron event, and the STM shifts from the tunneling regime into the field emission regime. As shown in Fig. 1, a high-bias (8–80 V) field emission mode can be utilized which has resolution of a few nm and a single-electron exposure mechanism which is roughly 3 orders of magnitude higher efficiency. However, in this mode, the atomic precision is lost, as the scatter of emitted electrons is much broader than the STM tip.

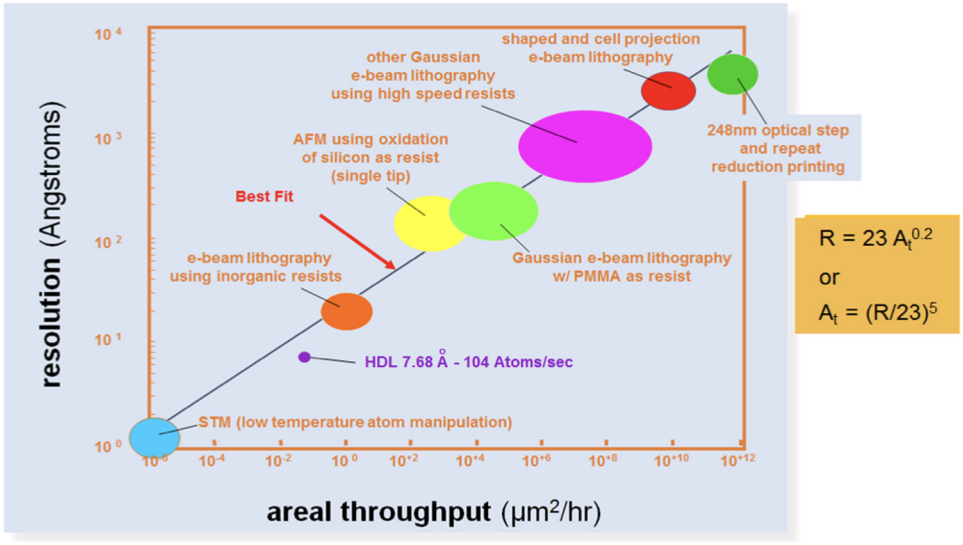
We have developed an STM controller[10] that is specifically designed to do HDL. This controller turns an STM into (in e-beam lithography terms) a Gaussian, variable spot size, vector scan lithography tool that is highly automated. While it has sub-nm resolution, its throughput with a single tip is very low, in the area of 104 surface Si atoms per second.

There are useful patterning applications for HDL even with a single tip. The potentially most impactful is patterning single donor spin-qubit quantum computing devices.[1] A similar process can be used for developing two dimensional (2D) quantum metamaterials.[2] We are also working to develop HDL patterned nanoimprint templates. However, all of these applications are limited by the very slow throughput of STM lithography.

III. TENNANT'S LAW

First published in 1999,[3] Don Tennant observed a trend in resolution versus areal throughput (At) for a wide variety of lithographic processes. The trend was that the throughput of a lithographic system varied with the fifth power of the resolution. Figure 5 is the graph from that publication. In an update in 2012,[4] this trend was shown to be valid primarily for serial writing lithographic tools. A subset of his data is shown with the best fit of the trend line which turns out to be R (Å) = 23*At (μm^2/h)$^{0.2}$.

In the case of HDL, using the surface area of 0.384 × 0.384 nm = 1.47 × 10^{-7} μm^2 as the surface area of an Si atom



From D.M. Tennant, Nanotechnology, (Springer-Verlag, New York, 1999)

FIG. 5. Tennant's law (Ref. 3) with an added data point for HDL. Reprinted with permission from D. M. Tennant, *Nanotechnology* (Springer-Verlag, New York, 1999), p. 164. Copyright 1999, Springer.

in the (100) plane and a rate of 104 atoms/s that we achieve with lithography conditions of +4 V sample bias, 2 nA set point current, and a scan rate of 20 nm/s, we can calculate an areal throughput of $5.5 \times 10^{-2}\,\mu m^2/h$.

We have inserted a data point based on the well-established resolution of HDL at 7.68 Å and our exposure rate of 104 atoms/s. Tennant's law predicts an areal throughput of $0.004\,\mu m^2/h$, which is "reasonably close" to our experimental value of $0.053\,\mu m^2/h$ (104 atoms/s).

We believe that by increasing the current and scan speed, we can improve the areal throughput by perhaps a factor of 10, and possibly higher. Furthermore, larger features can be exposed by the much more efficient field emission model.[7] However, it is clear that we cannot cheat Tennant's law by much with a single tip in the highest resolution mode. This fact will impose significant limitations to what can be accomplished with this patterning technology. Thus, we are driven to consider what we may be able to accomplish by going parallel.

IV. PARALLEL MEMS-BASED STM SCANNERS

The problem with taking current STM scanners parallel is that they use piezoelectric actuators whose inefficient conversion of applied voltage to displacement gives them both high resolution and large actuators. It is the size of the piezoelectric actuators that effectively precludes a large number of parallel scanners in a practical area.

MEMS actuation is of immediate interest because of the manufacturing infrastructure including CMOS foundries that manufacture MEMS,[11] the ability to integrate sensors as well as actuators, and the continued drive toward miniaturization. There are already MEMS-based scanning probe microscopes on the market.[12,13]

The basic architecture we envisage for an array of MEMS-based scanners is shown in Fig. 6, which is a 2D array of independent X, Y, and Z scanners where the XY footprint of each scanner is expected to be significantly larger than the XY scan area. In order to cover an entire area, there needs to be a global XY motion that is large enough to move the scan area of each MEMS scanner so that it can cover the area of at least the footprint of the scanner and allow stitching with the periphery of each of its neighboring scanners. We would want to achieve the highest density possible of scanners per unit area to maximize the throughput of the system to complete some relevant area.

Moreover, for the particular form of lithography that we are interested in parallelizing, atomically precise HDL, there is a requirement to align to the Si (100) 2×1 lattice. In particular, the standard method of exposing with atomic precision is to pass the tip along an Si dimer row which has a 0.768 nm spacing and the tip is required to be within ±0.1 nm of the center of the dimer row. With a single tip, it is easy to image and align to the dimer rows so that a given exposure area can be exposed with scans separated by 0.768 nm. However, when an array of tips is moved in unison, inevitable randomization of the relative tip apex positions at the nanometer scale will misalign many of the tips with respect to the dimer rows. This will demand a global raster with scans separated by 0.2 nm and most likely will require an even tighter pitch because of some global positioning errors. The end result will be a raster that will take at least four times longer to complete. For these reasons, in this paper, we will consider an array of XYZ scanners because we believe for most patterns a vector scan approach will provide more efficient exposure methods for HDL.

V. CHALLENGES TO PARALLELIZATION

A. Comparison to scaling conventional e-beam lithography

As mentioned previously, there have been a number of significant efforts to take conventional electron-beam lithography parallel and it is instructive to consider the difficulties that were encountered. A major problem faced by

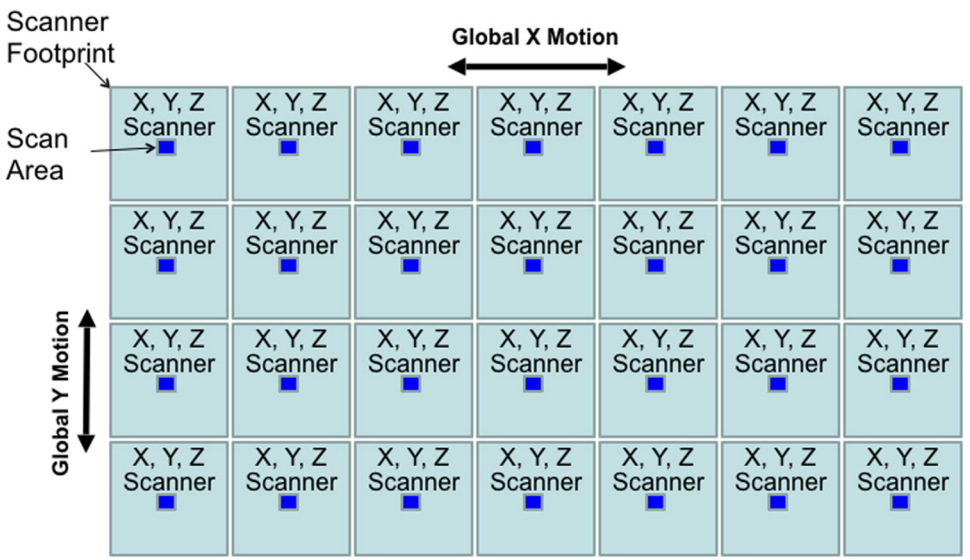


FIG. 6. MEMS scanner array architecture.

conventional electron-beam lithography is the Coulomb interaction of high current density (required for high throughput) beams interacting over the beam paths from source(s) to substrate.[14] These Coulomb interactions have been categorized into three effects: the space charge effect, trajectory displacement effect, and the Boersch effect. While correction for the space charge effect is technically feasible, the trajectory displacement and Boersch effects are statistical in nature and cannot be compensated for.[4] The scale of these problems increases exponentially as the number of closely spaced high current beamlets increases.

There is also the formidable wiring problem and the resulting cross talk of the many analog signals that must be sent into the beam-blanking/deflection array required to impose the pattern. The beam-blanking and/or deflection signals must be high frequency for a high throughput system and must be either high-voltage or high current to affect the high energy beamlets, exacerbating the cross talk problem. This problem is tractable for modest levels of parallelism, but the wiring/cross talk problem becomes extremely difficult as the number of beamlets to control increases.

While there are other challenges for MEMS-based scanners, in spite of the fact that HDL is a variation of e-beam lithography, the Coulomb interaction problem is essentially nonexistent. This is primarily because the beam paths are so short (a few nm at most) that the field lines from a neighboring tip/beamlet impart an inconsequential displacement of the beam from tip to sample. In the tunneling mode, there is actually no beam length since the electrons tunnel from the tip to the sample; so, there is essentially no opportunity to have their path altered by field lines in the vacuum. Other scanning probe lithography techniques that do not use charged particles for patterning similarly do not have a Coulomb interaction problem.

However, MEMS actuators also need analog signals to create their displacement motion. At first glance, the wiring problem appears even worse since there are three axes that need to be controlled and at least one return signal for HDL (the tunneling current) that is low current and susceptible to noise from cross talk from the other analog signals. This problem will get worse faster as parallelism increases than the case of arrays of beamlets in conventional e-beam lithography. However, this problem can be dramatically mitigated by not sending analog control signals into the array and sense signals out. The solution is to use mixed signal CMOS microcontrollers to run each (or a small cluster of) HDL scanners. Instead of the wiring and cross talk nightmare of running analog signals to each scanner in a large array, there would only need to be a power bus and a data bus routed through the array as depicted in Fig. 7.

As we have already developed a sophisticated software to run a single tip, we can estimate the size of a chip or the number of gates in an field programable gate array (FPGA) required to locally control a 3 DoF scanner.

B. Hardware implementation of the MEMS controller

Using microcontrollers to control the MEMS scanner not only has some distinct advantages but also has severe limitations exposed in this work. The main advantages are that they are easy to program and debug, thus, tremendously facilitate the implementation of the controller. Their main disadvantage is that their scalability is very limited. In this work, we require to drive a large number of controllers in parallel, and hence, we would require an array of microcontrollers. This would not only increase the complexity of the design but also the cost and power.

One alternative solution is to implement the controller in dedicated hardware. Creating a custom hardware design enables the system to be fully scalable by instantiating as many controller modules as MEMS controllers.

One typical way to create custom hardware designs is to analyze the software description of the controller running on

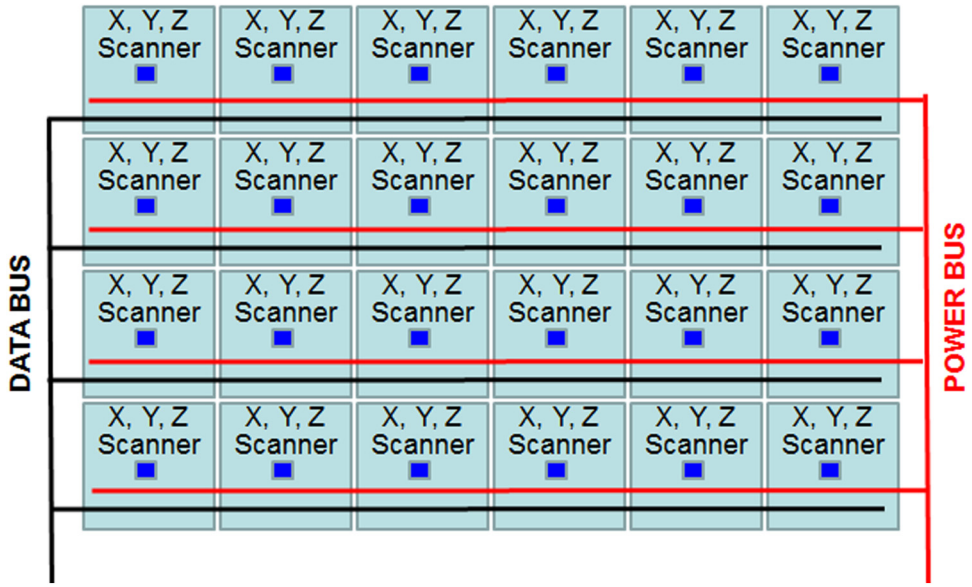


FIG. 7. Schematic depicting how an array of smart scanners can be powered and controlled by a power bus and data bus.

the microcontroller and implementing a hardware design that can execute its behavior using a hardware description language such as VERILOG or VHDL. This is time consuming and error prone. Thus, a new design methodology called high-level synthesis (HLS) that is starting to be used for commercial hardware designs was used in this work that can automatically convert behavioral descriptions into hardware.

HLS is the process that takes as input a behavioral, untimed description (e.g., ANSI-C or C++) and automatically generates an efficient hardware description that can execute it. This new technology seems ideal for this case because we already had described the MEMS controller in ANSI-C for the microcontroller. Thus, this code could be completely reused to be directly converted into hardware.

One additional advantage of using HLS is that we can retarget the code to either target a FPGA or an application specific integrated circuit (ASIC). This only requires to specify the target technology library, but the actual behavioral description is kept identical in both cases.

Figure 8 shows an overview of the complete flow. In this work, we used NEC's CyberWorkBench v 6.1 HLS[15] tool to synthesize the MEMS controller. In the output of this tool, a VERILOG description of the MEMS controller is in turn passed to either Intel's Quartus Prime[16] tools targeting an Arria V FPGA or to Synopsys Design Compiler[17] targeting an ASIC.

Table I shows the result after HLS and logic synthesis. The power is estimated using Intel's power play power estimator and Synopsys's power estimator for the FPGA and ASIC cases, respectively. From Table I, it can be observed that the FPGA consumes similar power as compared to the ASIC, although this is mainly because the ASIC operates at a clock frequency that is ~5.2× faster. When scaling down the ASIC's clock frequency to the same frequency as the FPGA, the power consumption drops also ~5 times. Hence, the ASIC is five times more power efficient. Although the FPGA is much slower than the ASIC, speed is not particularly relevant in this case because the controller modules are only required to work at 100 kHz. Nevertheless, a faster clock rate implies that less controller modules are potentially needed as these could be reused/time multiplexed. These result highlight some trade-offs between FPGAs and ASICs.

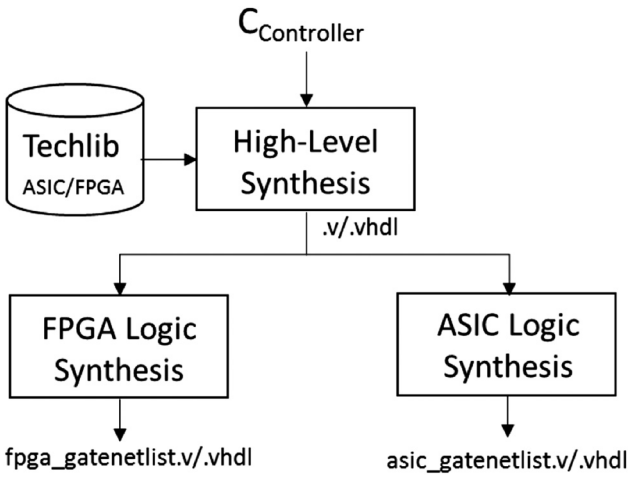


FIG. 8. Complete dedicated hardware flow overview.

In summary, this section shows that creating a dedicated MEMS controller is a feasible solution to address the scalability issues posed to control concurrently the array of controllers proposed in this work.

With this local microcontroller architecture, the wiring and cross talk issues are greatly simplified. Each smart scanner can receive high-level instructions about the pattern it is supposed to create and then use its local controller to do the patterning, inspect, and then report when it has completed its tasks. This simplifies greatly the problems encountered when increasing the level of parallelism. With the wiring problem greatly simplified and the Coulomb interaction essentially eliminated, scaling to larger numbers of scanners in an array becomes much easier than scaling conventional e-beam lithography.

C. Other scaling challenges

In the estimation of the authors, there are three significant challenges to scaling MEMS-based STM scanners that would execute HDL with large levels of parallelism.

Tip reliability and lifetime. One of the least reliable aspects of scanning tunneling microscopy is tip lifetime. Tips are constantly changing in major and minor ways. The minor changes are largely due to the quality of the vacuum and surface preparation. Atoms and molecules moving on or off and on the tip will change the manner in which the tip images and does lithography. Minor changes in the tips can potentially be dealt with by constantly monitoring the system and making adjustments in the imaging or lithography conditions to adjust for these changes. The frequency of minor changes can be reduced by improved sample and tip preparation as will be discussed later.

Major tip changes, on the other hand, are created by significant interactions between the tip and the sample surface. As seen in Fig. 9, major tip changes are not subtle events. These changes are not acceptable for HDL for a number of reasons: these tip sample interactions often change not only the tip but also the sample providing serious defects in the desired pattern. Even if the tip continues to be able to image and do lithography, the location of the primary tunneling point on the tip can be displaced by not insignificant distances. Furthermore, HDL's high-bias lithography mode is a field emission mode which is far more sensitive to tip shape than the tunneling mode, thus making significant physical changes of the tip unacceptable.

The cause of major tip crashes is a failure of the control loop that adjusts the tip's height. Occasionally, there are external perturbations such as mechanical or electrical perturbations that the control system is simply not capable of handling. However, relatively simple vibration isolation and/or active cancelation and electrical filtering can eliminate such external perturbations.

We have recently discovered that minor tip changes can destabilize the tip height control system causing major tip crashes.[18] Minor tip changes can affect the LBH that

TABLE I. Comparison of a single dedicated hardware MEMS controller implemented on an FPGA and ASIC.

FPGA					ASIC		
Area (Adaptive lookup tables)	Digital signal processing macros	BlockRAM (Mbits)	Power (mW)	Speed (MHz)	Area (μm^2)	Power (mW)	Speed (MHz)
2239	0	1820	30.3	189	52,109	26.65	987

strongly affects the gain of the proportional-integral (PI) control loop[18,19] that adjusts the tip height. The change in the gain can move the PI control loop into an unstable state so that small perturbations which would normally be handled by the control system now cause the system to oscillate and potentially crash which can in turn create a major tip change. We have developed a method where by modulating the set point current at a few kHz and monitoring the tip height response, an estimation of the LBH can be made and the operating parameters of the PI Loop can be adjusted dynamically, thus keeping the system in a stable, optimal regime and reducing the possibility of major tip changes.[19]

While more work needs to be done, we believe that through improved control systems and sample preparation, tip lifetime can be dramatically improved, as it must be, if reliable operation of a large array of tips is going to be practical.

Reliable tip preparation on MEMS scanners. Shortly after the invention of the STM, recognition of the importance of the tip structure led to numerous efforts to produce superior tips.[20,21] However, the inadequacy of the control systems to protect the tips largely frustrated these efforts because no matter how good the resulting tips were, their lifetime was so short that there was little value in the effort. Recently, however, several tip preparation methods have greatly improved the ability to routinely make either single atom apex tips[22,23] or at least very well controlled, very small radius of curvature tips.[24] There has also recently developed single crystal GaN nanowires that terminate in very small radius of curvature tips with very consistent tip shape.[25] Our experience with them demonstrates that they can image and do lithography similar to W tips. The advantages of the GaN tips are that they will be a much more consistent shape and that the GaN is much harder than W and covalently bonded so that there will be much less surface mobility of atoms even in very high field and current density encountered in HDL.

The problem remains of how to integrate STM tip preparation with MEMS processing and how to achieve tip placement within at least 100 nm of the desired location. We have already demonstrated a focused ion beam cut, pick, and place process that places GaN tips on metal surfaces.[25] We believe that finding a manufacturable process for STM tip on an MEMS scanner is an engineering task that is achievable.

Sample preparation. As mentioned above, sample preparation can affect tip changes, and like any lithographic procedure, the sample quality can affect the yield of the process. For research, it is permissible to look around and find an area that is satisfactory for the one or several patterns that need to be created. For manufacturing, the bar is much higher. There is also with HDL the need to deal with step edges that are (currently) inevitable. While single terraces of larger than $10 \times 10\,\mu m$ have been demonstrated, this has been accomplished by long high temperature anneals that produce step edge bunching in etched trenches.[26] On the other hand, step edges do not need to be eliminated, simply detected and adjusted to.[27] Sample preparation is another engineering task that can be solved when the perceived value is great enough to provide the resources required.

VI. DENSITY OF SCANNERS AND POSSIBLE LEVELS OF PARALLELISM

The final question is what levels of parallelism could be achieved with smart MEMS-based STM scanners that are capable of atomic precision HDL? This is an important technical and economic question that will affect whether this technology can become impactful. If we were targeting consumer electronics, which we are not, the relevant question would be how many scanners could operate in parallel on a 300 mm wafer? But the early nanotechnology products that HDL may address are most likely not going to be built on large Si wafers but instead on significantly smaller samples. What we will address is an estimation of the density of scanners that can be realistically achieved.

In what follows, we will not try to design a specific 3 DoF MEMS actuator in order to determine its size and therefore density in a given area. We will establish some high-level specifications and consider two different actuator choices to provide an array of smart MEMS STM scanners. The MEMS specifications are as follows:

- X and Y closed loop positioning with a range of at least $100\,nm \times 100\,nm$.
- Z closed loop positioning with a range of at least $5\,\mu m$ and a stiffness of at least 25 N m to avoid electrostatic pull-in between the tip and the sample.
- Fundamental resonant frequencies of at least 5 kHz.

A scan range of $100\,nm \times 100\,nm$ is quite small but would still take longer than 1 min to expose entirely with equal line space patterns in the AP mode at our current highest exposure rate of 104 atoms/s. The time to do a global move and resume exposing should be on the order of a second, and the increase in density of tips clearly favors a scan field of this magnitude.

In a 2D array, the density of tips will be determined by the area of the MEMS device in the 2D plane. The required range and stiffness in the direction of motion will affect the

size of the MEMS actuator that will achieve the stiffness and range specifications. Also, in general, it is more difficult to obtain large motions with MEMS actuators out of the plane of the substrate. Because the stiffness and range specifications are much larger in the Z axis (normal to the substrate to be patterned), an MEMS design with the Z axis parallel to the MEMS substrate would be advantageous. Therefore, we will investigate in this paper, a 3 DoF MEMS device with the X and Z axes in plane and the Y axis out of plane.

While there are a number of other choices for MEMS actuators, the two that we will consider are electrothermal and electrostatic actuators. The electrothermal actuators are attractive from the point of view that they produce considerably more force than electrostatic actuators of similar dimensions when practical voltages are applied. The greater force translates to smaller sized actuators for a given range of motion. With a fairly crude assumption, we are going to estimate that the actuator size to range of motion is roughly 200:1 for electrothermal actuators and 1000:1 for electrostatic actuators. This ratio is important because it will impact the area of the MEMS STM scanner. Let us assume that the Z axis actuator and the X axis actuator maximum sizes are both in the direction of their respective axes of motion and that the out of plane Y axis actuator is orthogonal to the axis of motion and its maximum size is in the Z axis. See Fig. 10 for such an example. In this case, the relevant width of the MEMS scanner will be the product of the required scan range and the size-to-range ratio of the selected MEMS actuator. The other dimension in the plane of the tip array will be the sum of the MEMS device thickness plus the MEMS substrate thickness. A single MEMS device with electrostatic actuators is depicted in Fig. 10, where the Z actuators sit on the 10 μm thick device layer platform suspended on the Y, X flexures. The Y motion is achieved by the Y control beams tilting the platform and the X motion by the lateral motion of the platform.

If we assume a substrate thickness of 50 μm and a total MEMS device thickness of 30 μm allowing for some clearance above the MEMS device, we have one dimension of the MEMS STM scanner footprint in the array of tips of 80 μm. The other dimension will be the product of the scan size and the actuator size to range ratio. We will also consider an additional 10 μm boundary between scanners to allow some assembly structure. The footprint of an MEMS scanner in this configuration is given by Eq. (4)

$$F_p = (A_r X_r + B)(S_t + M_t), \tag{4}$$

where F_p is the MEMS footprint area, A_r is the actuator ratio of size to range, X_r is the X range of the scanner, B is an MEMS border, S_t is the substrate thickness, and M_t is the MEMS thickness. The density of scanners per cm^2 could be given as $1/F_p$ with F_p given in cm^2.

The MEMS chip area is given by Eq. (5)

$$\mathrm{Ca} = (A_r X_r + B)(A_r Z_r + B), \tag{5}$$

where Z_r is the Z range of the scanner.

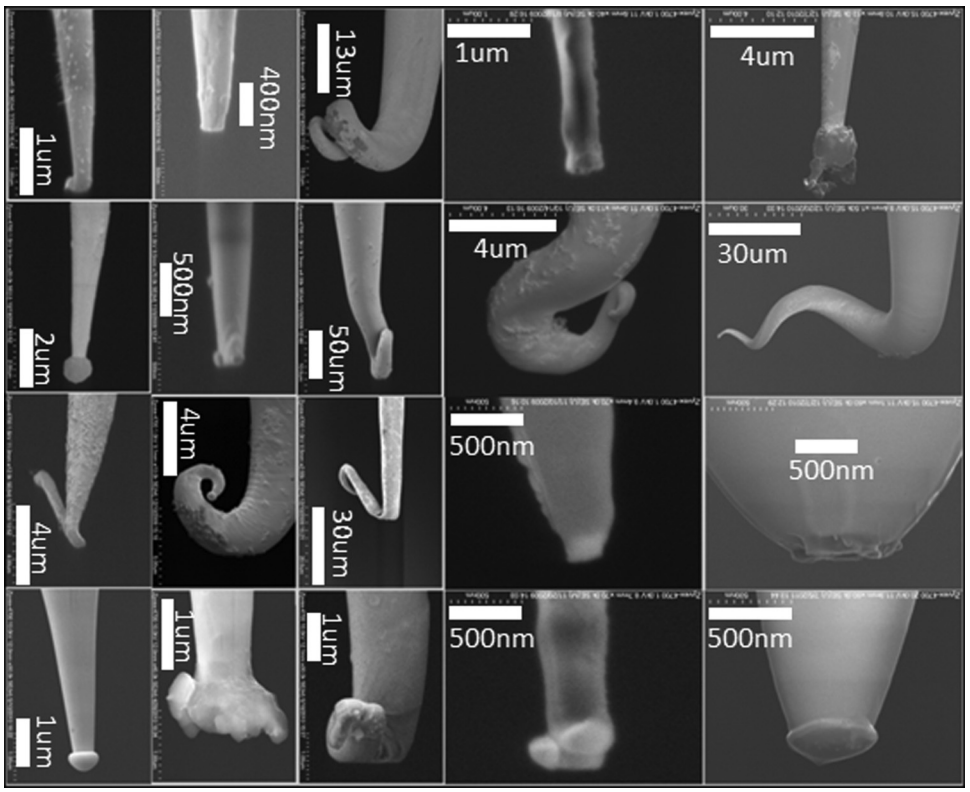


FIG. 9. Collection of scanning electron microscope images of tips that have crashed into Si samples in our ultrahigh vacuum STM systems.

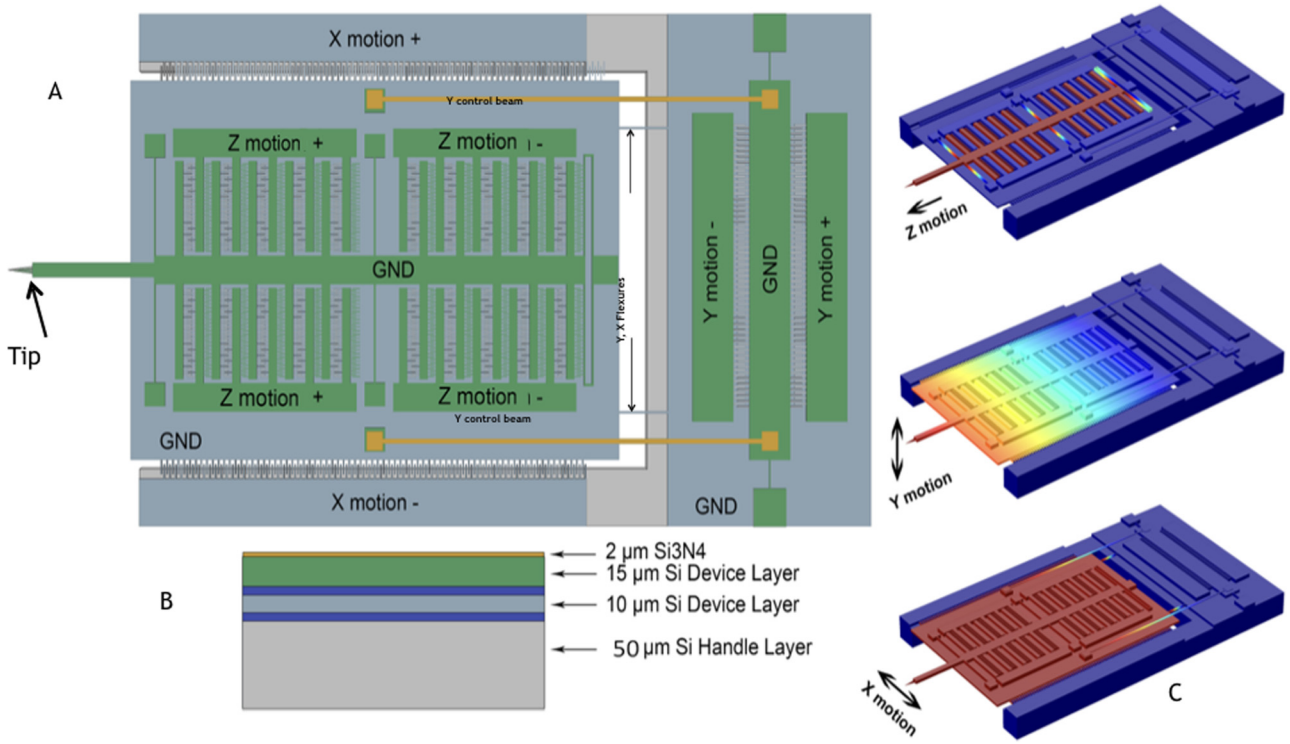


FIG. 10. Conceptual electrostatic 3 DoF MEMS device. (a) The plan view of the device showing the comb drives for the three axes, (b) shows the cross section of the layered structure, (c) depicts motion in each of the three axes. The Z and X motion are in plane of the MEMS device and the Y motion is a tilt out of plane that would achieve a range of 100 nm. This is a conceptual design only, is not optimized, and could be executed with electrothermal linear actuators as well.

The time to expose the scan field in a worst case of equal lines and spaces with the AP mode is given by Eq. (6),

$$T_{sf} = A_t X_r Y_r + N_t, \tag{6}$$

where A_t is the areal throughput, Y_r is the Y scanner range, and N_t is a percentage of the raw exposure time as an overhead to navigate the scan field.

The time required to completely expose a substrate made up of any number of MEMS scanners whose combined footprints equal the area of the substrate is given by Eq. (7),

$$T_{sub} = \frac{T_{sf} F_p}{X_r Y_r}, \tag{7}$$

where T_{sub} is the time required to completely expose the substrate of any size that is covered by an array of MEMS scanners. T_{sub} should not be taken as a realistic estimation of the time to expose a given substrate because it is a worst case scenario, but it is a worthwhile figure of merit.

With these equations for the configuration described above with the assumption of $S_t = 50\,\mu$m, $M_t = 30\,\mu$m, $B = 5\,\mu$m, $X_r = 100$ nm, $Y_r = 100$ nm, and $Z_r = 5\,\mu$m, we can calculate the density of tips and the chip area for

- Electrothermal actuators with 200:1 size to range:
  - 37 037 tips/cm^2
  - MEMS chip area = 30 000 μm^2
- Electrostatic actuators with 1000:1 size to range:
  - 10 101 tips/cm^2
  - Chip area = 550 000 μm^2

While the 37 037 tips/cm^2 for the electrothermal actuators is a very high level of parallelism, there are two significant problems for electrothermal actuators. The first is the varying thermal load depending on the active motion of the positioning of the scanner. As the patterns being carried out by the different scanners are in general dissimilar, the heat generated will vary both spatially and temporally. The varying thermal load will create fluctuating thermal gradients that will create thermal drift that will be difficult to correct with the usual sensors for closing the loop on such a local scale. Sarkar has largely eliminated the time varying thermal load by designing actuators that are constantly dissipating a constant amount of heat regardless of what the actuators are doing.[28] To first order, this eliminates the time varying thermal gradients but increases the total heat load that must be removed from the scanner array. Additionally, the chips will be sandwiched together providing a poor thermal path to remove the heat. This problem further is compounded by the fact that HDL is executed in vacuum. While the heat flow problem may be solvable, we will cease considering electrothermal actuators and will continue to explore electrostatic MEMS actuators.

While the calculated density of 10 101 tips/cm^2 for electrostatic MEMS is certainly lower than that of electrothermal MEMS, it is still a significant level of parallelism. This

TABLE II. Sensitivity analysis for design factors in MEMS STM scanners to be used in an array.

	X_r, Y_r scan (nm)	A_r size ratio	S_t substrate (mm)	M_t MEMS (mm)	A_t exposure (ms/atom)	N_t exposure overhead	Figure of merit
Value	100	1000	50	30	9.6	1%	90563
Improvement with 10% change (%)	9.89	9.89	5.93	3.41	11.11	0.01	

density would yield 65 168 tips in a 1 in.^{2} area, 793 330 tips in the area of a 100 mm wafer, and 7 139 970 tips in the area of a 300 mm wafer.

Using these same assumptions and our current exposure rate of 9.6 ms/atom, we can calculate T_{sub} as a figure of merit and measure the sensitivity of this figure of merit to 10% improvements in X_r, Y_r, A_r, S_t, M_t, A_t, and N_t. The results are shown in Table II.

For the nominal design listed above, the potenial levels of parallelism achieved by larger arrays with the same tip denisty are plotted as data points in Fig. 11.

The task to assemble the array from separate chips will be nontrivial, especially with respect to keeping the tips to within a relatively small tolerance of the ideal grid. As described above, we have estimated that an FPGA controller would require on the order of 50 696 μm^2, since this is only ~10% of the area required by the MEMS actuators required to control a single tip integrating the control electronics with the MEMS either with homogeneous ASIC integration or a heterogeneous assembly integration with Quilt-packaging[29] or other process. The heterogeneous assembly would have the advantage of better thermal isolation of the control electronics from the MEMS actuators. Good thermal contact to the back of the array will be essential as the heat transfer will have to account for ~300 W/cm^2 based on the power per controller estimate at ~30 mW per scanner. While not a trivial heat flow problem, active cooling should be able to remove the heat generated by the control electronics.

The task to assemble the array from separate chips will be nontrivial, especially with respect to keeping the tips to within a relatively small tolerance of the ideal grid. All of this is nontrivial but potentially doable with sufficient resources.

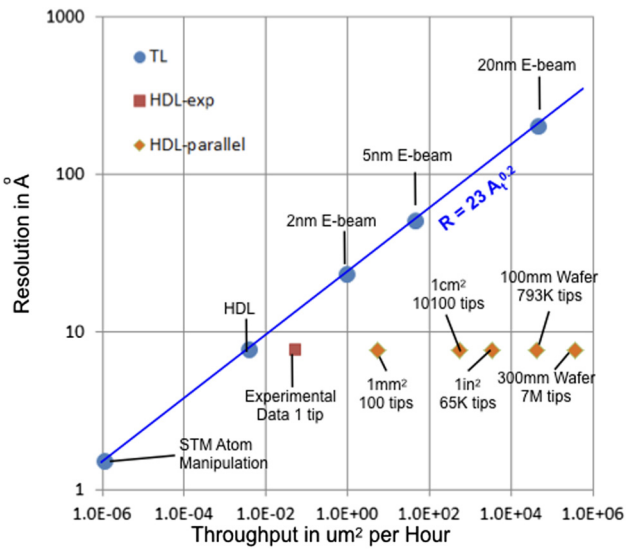


FIG. 11. Subset of Tennant's law where well-established data points for the areal throughput vs resolution for conventional e-beam lithography and atom manipulation with an STM are compared with one experimental point for HDL and some speculative points for HDL that maintain the 7.68 Å resolution while maintaining the calculated density of 10 101 tips/cm^2 with increasing array size which increases the areal throughput via parallelism.

VII. DISCUSSION AND CONCLUSIONS

Serial write lithography tools have significant advantages in that they do not require masks and they typically have very high resolution. This is certainly true of hydrogen depassivation lithography which is a nonconventional type of e-beam lithography which has sub-nm resolution. However, as demanded by Tennant's law,[3,4] its high resolution is burdened by extremely low areal throughput. Fortunately, two of the main impediments to taking conventional e-beam lithography parallel—(1) Coulomb interactions of the electron beams and (2) the wiring/cross talk problems presented by sending high current or voltage analog signals into a large array to control the beamlets—are greatly mitigated by HDL using smart MEMS scanners. While the reliability requirements for each scanner will need to rise as the level of parallelism does, the wiring and beam interaction difficulties will not increase exponentially in difficulty as they would in conventional e-beam lithography. We have estimated that electrothermal actuators in MEMS may be able to achieve densities of 10 101 three DoF STM scanners per cm^2 with a 100 nm × 100 nm scan field. This density could achieve on the order of 7×10^6 scanners in the area of a 300 mm wafer.

Even greater density of 3 DoF electrostatic MEMS may be possible as suggested in a Bell Labs publication[30] where a 200 × 200 μm footprint MEMS device was developed that had two tip-tilt axes (>±3°) and a piston action of 5 μm.[30] A tip shaft 10 μm long with the base of the shaft at the tip-tilt axis would allow a scan area of 1 μm^2. This small MEMS scanners would support a 2500 tips/cm^2 array density. The published design is probably not suitable for an STM scanner, but it does demonstrate that even a decade ago with significant resources, very small footprint electrostatic MEMS can achieve 10× our desired range of motion, suggesting that there is room for miniaturization beyond what we have estimated, potentially leading to higher densities.

There are significant engineering problems to be overcome if a large level of HDL parallelism is to be achieved.

In our opinion, it is a major advantage that the majority of the engineering problems reside in the domain of micro- and nanofabrication. The scaled MEMS devices and mixed signal ASICs required for a large array simply require a relatively large commitment of resources. Sadly, the resources will not be motivated by HDL as the lithography replaces the deep UV or extreme ultraviolet lithography for consumer electronics. Let us state again that, even with over $7 \times 10\text{^}6$ tips operating in parallel on a 300 mm wafer, HDL is many orders of magnitude too slow for consumer electronics. However, there are already technologies that will be enabled by the resolution and precision of HDL such as analog quantum simulation devices[2] and quantum computing[1] that are possible initially even with a single STM scanner. We believe that success in these and other emerging technologies will make available the resources to push down this smart MEMS path to HDL parallelism. While we have focused on our interest in atomic precision HDL, we believe this path to scanning probe parallelism will find many other applications in other forms of direct lithography, mask/template making, assembly, inspection, and metrology.

Future work will involve trying to develop an optimized 3 DoF MEMS scanner, further exploring the requirements of the FPGA microcontrollers and a more in-depth consideration of the packaging and integration issues including the thermal loads required. The sensitivity analysis in Table II suggests that reducing the scan size, the size to range ratio, and the exposure rate would be the most effective at improving the figure of merit. However, reductions in both the scan size and the size to range ratio will increase the thermal load problem. Improving the exposure rate would come with little or no increase in thermal problems.

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[1]M. Y. Simmons, *2015 IEDM*, Washington DC (IEEE, New York, 2015), pp. 1.2.1–1.2.4.
[2]*Workshop on 2D Quantum MetaMaterials*, 25–26 April, edited by H. G. Owen and W. Kirk (NIST, Gaithersburg, MD, 2018).
[3]D. M. Tennant, *Nanotechnology* (Springer-Verlag, New York, 1999), p. 164.
[4]D. M. Tennant, J. Vac. Sci. Technol. A **31**, 050813 (2013).
[5]J. N. Randall, J. W. Lyding, S. Schmucker, J. R. Von Ehr, J. Ballard, R. Saini, and Y. Ding, J. Vac. Sci. Technol. B **27**, 2764 (2009).
[6]J. N. Randall, J. B. Ballard, J. W. Lyding, S. Schmucker, J. R. Von Ehr, R. Saini, H. Xu, and Y. Ding, Microelectron. Eng. **87**, 955 (2010).
[7]J. B. Ballard, T. W. Sisson, J. H. G. Owen, W. R. Owen, E. Fuchs, J. Alexander, J. N. Randall, and J. R. Von Ehr, J. Vac. Sci. Technol. B **31**, 06FC01 (2013).
[8]See: http://www2.fkf.mpg.de/ga/research/stmtutor/stmtheo.html.
[9]E. Foley, A. Kam, J. Lyding, and P. Avouris, Phys. Rev. Lett. **80**, 1336 (1998).
[10]See: https://www.zyvexlabs.com/apm/products/zyvector/.
[11]C. M. Liu *et al.*, *2011 16th International Solid-State Sensors, Actuators Microsystems Conference*, Beijing, China (IEEE, New York, 2011), pp. 807–810.
[12]N. Sarkar, R. R. Mansour, O. Patange, and K. Trainor, Transducers **2011**, 2610 (2011).
[13]See: https://www.icspicorp.com/.
[14]J. A. Liddle, M. I. Blakey, C. S. Knurek, M. M. Mkrtchyan, A. E. Novembre, L. Ocola, T. Saunders, and W. K. Waskiewicz, Microelectron. Eng. **41–42**, 155 (1998).
[15]NEC Corporation, CyberWorkBench, v.6.1.
[16]Intel, Quartus Prime.
[17]Synopsys, Design Compiler.
[18]F. Tajaddodianfar, S. O. R. Moheimani, J. Owen, and J. N. Randall, Rev. Sci. Instrum. **89**, 013701 (2018).
[19]F. Tajaddodianfar, S. O. R. Moheimani, and J. N. Randall, IEEE Trans. Control Syst. Technol. **1**, 1 (2018).
[20]H.-W. Fink, IBM J. Res. Dev. **30**, 460 (1986).
[21]P. K. Hansma and J. Tersoff, J. Appl. Phys. **61**, R1 (1987).
[22]M. Rezeq, J. Pitters, and R. Wolkow, J. Chem. Phys. **124**, 204716 (2006).
[23]H. S. Kuo, I. S. Hwang, T. Y. Fu, Y. C. Lin, C. C. Chang, and T. T. Tsong, Jpn. J. Appl. Phys. **45**, 8972 (2006).
[24]S. W. Schmucker *et al.*, Nat. Commun. **3**, 935 (2012).
[25]S. Brueck, International Patent Application No. PCT/US2017/029180 (24 April 2017).
[26]K. Li, N. Pradeep, S. Chikkamaranahalli, G. Stan, R. Attota, J. Fu, and R. Silver, J. Vac. Sci. Technol. B **29**, 041806 (2011).
[27]J. N. Randall, U.S. patent 9,329,201 (15 March 2013).
[28]N. Sarkar, U.S. patent 9,267,962 (23 February 2016).
[29]G. H. Bernstein, Q. Liu, M. Yan, Z. Sun, D. Kopp, W. Porod, G. Snider, and P. Fay, IEEE Trans. Adv. Packag. **30**, 731 (2007).
[30]F. Pardo *et al.*, *IEEE/LEOS International Conference on Optical MEMS and Their Applications*, Big Sky, MT, 21–24 August 2006 (IEEE, New York, 2006).